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The Formation of Lateral Interconnections Extending over 100-μm-Thick Chips

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1. Introduction

Recently, the increased markets on wireless communications and automobiles require packaging various functional LSI-chips and MEMS components, which are produced in incompatible processes. For that reason, hetero-integrated packaging (HiP) technology is expected to be a promising board level integration technique, which can integrate MEMS devices and LSI chips by lateral interconnections or micro-bumps, known as face-up or face-down types, respectively[1,2]. Figure 1 shows a conceptual viewgraph of Cu high-step-coverage lateral interconnections over a thick Si-chip for the highly integrated MEMS devices and LSI chips application.

However, the large height difference between the chip and a supporting wafer always causes problems, such as difficulties in transferring mask pattern to samples due to the different depth-of-fields in photolithography and a low coverage of each layer on chip lateral side. These problems of high topography step were often reported in the process of forming micro parts in MEMS. Further, the formation of uniform thickness of Cu seed layer/Ta barrier layer on the lateral side of the thick chip for the selective Cu electroplating is also highly important to realize the board level integration.

Here we (i) show the formation of high-step-coverage lateral Cu interconnections extending over the 100 μm thick chips of MEMS and passive devices; (ii) present the electrical resistivity data of successfully fabricated Cu lateral interconnections over 100 μm thick Si-chips.

2. Experimental

Process flow for the test chip fabrication, self-assembly of the chips and the Cu lateral interconnections over the chip is schematically shown in Fig. 2. 100-μm-thick test chips were produced from thermally oxidized Si wafers by standard photolithography, etching and chemical mechanical polishing. In the self-assembly process, the test chips were assembled onto Si wafers, and then, SiO_2 dielectric layer and Cu seed layer/Ta barrier layer were formed by using Plasma CVD and RF sputter, respectively. Finally, the selective area Cu metallization was formed by patterning a thick photoresist followed by Cu electroplating.

Successfully fabricated Cu interconnections were analyzed for their microstructure and electrical characteristics by using field emission scanning electron microscope (FE-SEM) and Agilent 4156C semiconductor parameter analyzer, respectively.

3. Results and discussion

Fig. 3 shows cross-sectional view of 20 μm thick photoresist spin-coated on a 100-μm-thick chip. It has a acceptable coverage at the edge and the corner of chip step after spin-coating and soft bake.

Lithography results are shown in Fig. 4, where the original sizes of mask line pattern are 4 μm, 6 μm, 8 μm and 10 μm. It is found that the exposure dose over 3000 mJ/cm^2 (typical mercury lamp, I-line) was well enough to sensitize the photoresist at the bottom corner of Si-chip. However, SEM images shown in Fig. 5 reveal the sizes of Cu interconnections, against the original mask line widths, widen to 36 μm, 42 μm, 48 μm and 58 μm, respectively. Moreover, it is observed that the width of fabricated interconnections is also spatially different. As seen in Fig.5a, line widths on chip surface and bottom corner of chip are respectively, 36 μm and 25 μm. It might be arising from the difference in the photoresist thicknesses, as seen in Fig. 3b.

Fig. 6 shows SEM cross-sectional views of the proposed Cu interconnection structure (a) extending from wafer to chip surface, (b) on the chip surface, (c) of the chip's bottom corner and (d) the upper corner of the chip. The coverage ratios (thickness on the chip's surface divided by those on the chip's lateral side) for each formed layer are, 3:1, 3:1, 1.5:1, 1:1 for Ta barrier layer, Cu seed layer, Plasma CVD SiO_2 layer and the electroplated Cu layer. The electrical resistance (as shown in Fig. 7) are approximately 31.1mΩ and 24mΩ respectively for 4μm × 2000μm and 10μm × 2000μm of Cu interconnection line. From this, it is inferred that the resistance deviation for Cu lateral interconnections were lower than 5%.

4. Conclusions

Cu high-step-coverage of lateral interconnections extending over Si-chip was successfully fabricated. The existing high topography step was having only a small influence on the lateral coverage of Cu interconnections.

Acknowledgments

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References

[1] T. Fukushima *et al.*, IEDM Tech. Dig., pp. 359-362 (2005).
[2] T. Fukushima *et al.*, IEDM Tech. Dig., pp. 985-988 (2007).

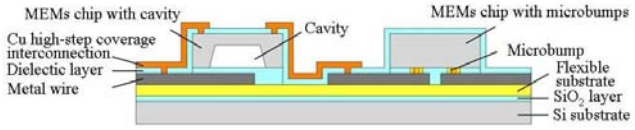

Fig. 1 Conceptual viewgraph of system with a lateral interconnections extending over MEMS and LSI chips on the Si-wafer.

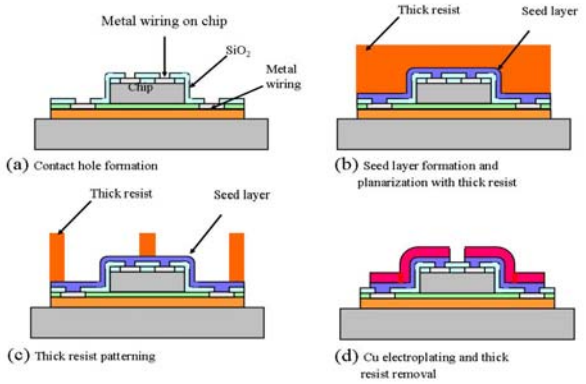

Fig. 2 Process flow for high-step-coverage Cu lateral interconnections with self-assembly of Si chips.

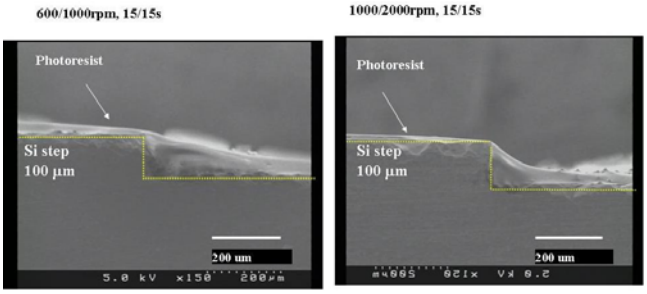

Fig.3 FE-SEM cross-sectional view of spin-coated photoresist with self-assembled 100mm thick chips on the Si wafer.

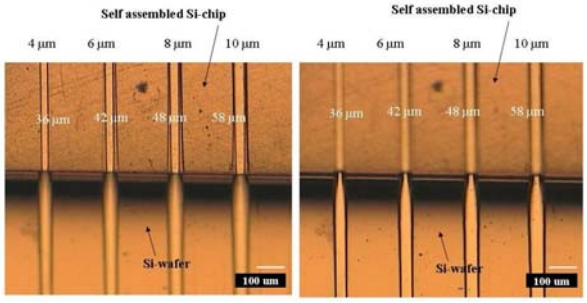

Fig. 4 Microscopy images of lithography patterns (a) with focus on Si-Chip and (b) with focus on Si-wafer.

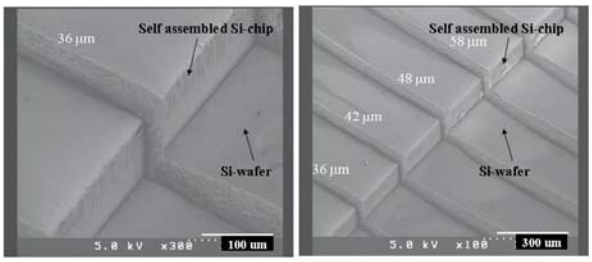

Fig.5 FE-SEM cross-sectional view of fabricated Cu high-step lateral interconnections over a self-assembled test chip on the Si-wafer.

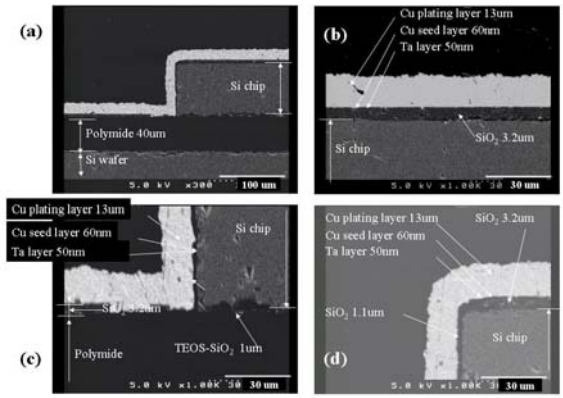

Fig. 6 FE-SEM cross-sectional views of Cu high-step lateral interconnection with Cu seed layer/Ta barrier layer/SiO_2 dielectric layer/Si substrate structure.

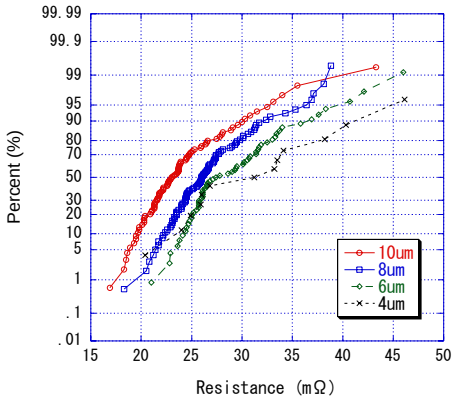

Fig.7 Measured resistance of Cu high-step lateral interconnetions formed over self assembled Si-chip on the Si-wafer.