Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 486-487

P-5-8

Low Gate Charge Power VDMOSFETs with Dual-Gate Floating NP Well Design

Chien-Nan Liao[1], Feng-Tso Chien[2] and Yao-Tsung Tsai[1]

[1] Dept. of Electrical Engineering, National Central University, Jhongli 32001, Taiwan
TEL：+886-4-24517250 ext.4936 E-mail：955401011@cc.ncu.edu.tw
[2]Dep. of Electronic Engineering, Feng Chia University, Taichung, Taiwan

1. Introduction

Power Vertical Double-diffused Metal Oxide Semiconductor FETs (VDMOSFETs) are widely used as a switch in many fields such as converter, controller and inverter[1-2]. Comparing to the bipolar junction transistor (BJT), the VDMOSFETs attract a large attention because of its advantages: high input impendence, thermal stability, superior switching performance and large safe operation area (S.O.A.)[2-4].

The switching loss occupies a large part of the total power loss of a power VDMOSFET during high-power RF operating [5]. Low switching loss device can be carried out by reducing the gate-drain charge (Q_{GD}) which is effected by the gate-drain overlap area. One way to reduce the switching loss is to shorten the gate length between the adjacent wells to reduce the gate-drain overlap area. However, high on-resistance (R_{ON}) will occur because of the parasitic junction FET (JFET) effect which results from the adjacent wells region. Therefore, a device figure of merit (F.O.M.) can be defined as the product of $R_{ON} \times Q_{GD}$ for a specified breakdown voltage (V_{BR})[6-7].

Other approaches such as the Self-aligned Terraced-Gate MOSFET (STGMOSFET) and Dual-Gate MOSFET (DGMOSFET) had been reported to reduce the gate-drain charge by increasing the gate oxide thickness or removing part of the gate-drain overlap area[8-11]. The DG structure suffers a high electric field region at the edge of the removed gate and sacrifices the V_{BR}[12]. Therefore, a thicker or a higher resistance epi-layer is needed to maintain breakdown voltage, but a high R_{ON} and high conduction loss occur at the same time. Consequently, a floating p-region was added between the DG structure to relax the electric field crowding effect[13]. However, the added floating p-region causes the R_{ON} to increase rapidly. To overcome the problem, a DGMOSFET with npn-region was proposed to reduce the high R_{ON}[14]. However, it leads to a high electric field at the interface between gate oxide and semiconductor which might cause the oxide breakdown and reliability issue. In addition, the structure proposal in [14] needs additional masks and increases possible lithography misalignment during process.

In this study, we propose a new cell structure which contains a DG structure and np-well to realize a low Q_G device without complex process flow and overcome the problems mentioned above. The main features of the new cell structure are the reduction of the Q_{GD} by partial gate area removal and avoiding electric field crowding by the additional floating np-well.

2. Device Fabrication

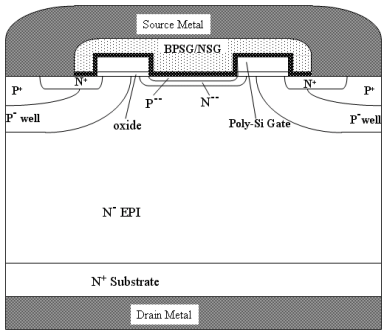


Fig. 1 The cross-section view of the proposed structure.

Fig. 1 shows cross-section of the proposed power VDMOSFET. The epitaxial layer (Epi) we use here have a resistivity of 6 Ω-cm with a thickness of 15 μm, which is designed for 200V devices. After field oxide was defined the device size and termination structure. A gate oxide and poly-silicon was deposited, respectively. The well and source masks were used to define the p-well (B_{11} @ 5×10^{13} cm^{-2}) and source-well (As @ 5×10^{15} cm^{-2}), respectively. The DG structure was formed after source implantation. Then, B_{11} (1.7×10^{12} cm^{-2}) was implanted after P (1×10^{12} cm^{-2}) to form the floating np-well. Although the added implantation was also doped into the well region, the concentration can be ignored comparing with that in the well. Here, we used a matrix mask to fabricate the conventional and proposed devices to prevent process vibrations. The gate length and the cell pitch of the conventional and proposed structure are 11 μm and 15 μm, respectively.

3. The Results and Discussion

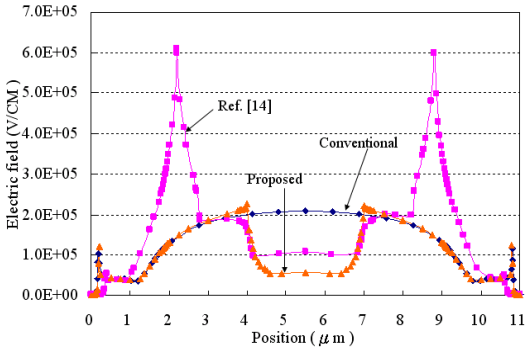
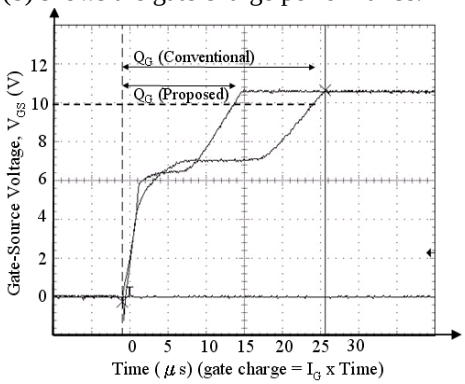


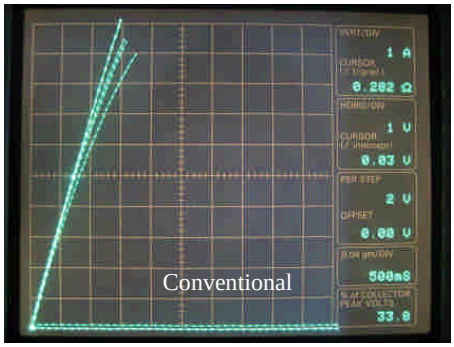
Fig. 2. The surface electric field distribution of the conventional, the device proposed in [14] and the proposed structure.

We simulated the surface electric field of the conventional, the device proposed in [14] and our proposed structure by ISE-TCAD[15]. Fig. 2 shows the surface electric

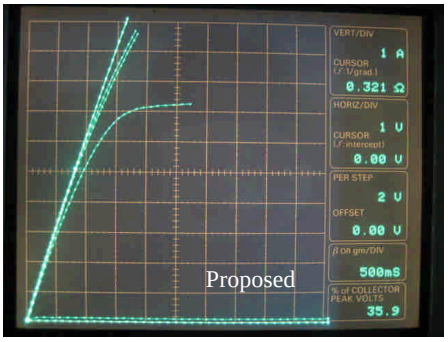
field distribution of all devices. It can be seen that the surface electric field is very high of the structure in [14] than the others. Similar surface electric field distribution can be found in [14] and other DG structure[12]. This phenomenon will lead to oxide breakdown and reliability problem. The DGMOSFET with floating np-well structure not only reduce the Q_{GD} by partial gate area removal but also overcome the high electric field peak problem. Fig. 3 (a) shows a top view photograph of the proposed device. Fig. 3 (b) shows the gate charge performance.



(a)



(b)



(c)

Fig. 3 (a) The measured gate charge performance and (b) the measured on-resistance of the conventional and proposed devices.

The Q_G curves were tested under the conditions of V_{DD} = 160 V and I_D = 6 A with the gate bias current (I_G) of 1 mA. The Q_{GD} (Q_G) of the proposed device decreases from 15.7 nC (25 nC) to 5.9 nC (14.8 nC) at V_{GS} = 10 V, respectively. The R_{ON} was tested by the *KEITHLEY* 371A under the conditions of I_D = 6 A and V_{GS} = 10 V. The R_{ON} increases slightly from 282 mΩ to 321 mΩ. That is because the small p-region occurs additional JFET effect. The trade off of the concentrations of the n-region and p-region are the key design issues in this DGMOSFET with floating np-well structure. An unproper dosage for the n and p region will result in a lower breakdown voltage or higher on-resistance. Tab. 1 lists the device characteristics of the conventional and the DGMOSFET with floating np-well structure. The breakdown voltage of the proposed structure can be maintained over 230 V. In spite of the slightly increased R_{ON}, the F.O.M. of the DGMOSFET with floating np-well is 42.8 % of the conventional due to a much lower gate charge performance. A lower F.O.M. is helpful to improve device performance.

	Q_{GD} (nC)	Q_G (nC)	R_{ON} (mΩ)	F.O.M. (nC x mΩ)
Conventional	15.7	25	282	4427.4
Proposed	5.9	14.8	321	1893.9

Table 1 Comparison of the electrical characteristics of the conventional and the proposed structure. The number in the brackets is the value normalized to conventional.

4. Conclusion

In this study, we propose the DGMOSFET with floating np-well power VDMOSFET to improve device performance. A part of the gate area of the conventional device is removed to form the DG structure. Then the np-well is formed to avoid premature breakdown without sacrificing too much on-resistance. Although the on-resistance will increase slightly, the Q_{GD} and F.O.M. of the proposed device are 37.6 % and 42.8 %, respectively, of the conventional structure. It is benefit for improving switching speed and switching loss of the power VDMOSFETs.

5. References

[1] M. H. Rashid, POWER ELECTRONICS CIRCUITS, DEVICES, and APPLICATIONS (2004).

[2] D. A. Grant and J. Gowar, POWER MOSFETS Theory and Applications (1989).

[3] B. J. Baliga, *IEEE Trans. Electron Devices* **10** (1996) 1717

[4] B. J. Baliga, *IEEE Trans. Electron Devices* **6** (1991) 1568

[5] Z. J. Shen, Y. Xiong, X. Cheng, Y. Fu, and P. Kumar, *IEEE Industry Applications Conference* (2006) 1438

[6] F. T. Chien, M. H. Lai, S. T. Su, K. W. Tu, and C. L. Cheng, *IEICE Trans. Electron.* (2005) 694

[7] A.Q. Huang, *IEEE Electron Devices Lett.*. **5** (2004).298

[8] D. UEDA, H. TAKAGI, and G. KANO, *IEEE Trans. Electron Devices* **4** (1984) 416

[9] B. J. Baliga, Power MOSFET Semiconductor (1996)

[10] H. Ikeda, H. Yoshida, and T. Onikura, *IEDM Tech. Dig.* (1982) 246

[11] Y. Shimada, K. Kato, S. Ikeda, and H. Yoshida, *IEEE Trans. Electron Devices* **8** (1982) 1332

[12] S. Xu, K. P. Gan, P. D. Foo, Y. Su, and Y. Liu, *IEEE Electron Devices Lett.* **4** (2004) 176

[13] T. Sakai and N. Murakami, *IEEE Trans. Electron Devices* **7** (1989) 1381

[14] W. Chen, B. Zhang, and Z. Li, *Semicond. Sci. Technol.* **22.** (2007) 1033

[15] *ISE TCAD Manuals*, release 8.5