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A Novel Match-line Charging Control Scheme with a New Sense Amplifier for High-Speed and Low-Power Content-Addressable Memory

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1. Introduction

Content-addressable memory (CAM) is a storage device that searches for the matching data by content and returns the address of the matching data. Due to the rising demand of CAM for high speed search capability in various applications, the size as well as power consumption of CAM arrays continue to rise.

A lot of researches have been done to reduce the power consumption and to increase the speed. Previous works present some schemes such as selective-precharge scheme [1], current-race scheme [2], current-saving scheme [3], [4], etc. It is reported in a survey [5] that the current-saving scheme consumes less power than other schemes [1], [2], [6]. In this paper, we proposed a simplified match-line charging control scheme. Comparison with the current-race and current-saving schemes shows match-line energy reduction of over 50% and speed improvement of over 3 times.

2. Proposed Charge Controlling Scheme

Fig. 1(a) shows the basic architecture of the proposed charge controlling scheme. Here, the array of CAM cells stores the data entries; search data register stores the search word; each charge controller block controls the charging and discharging process of the respective match-line (ML); and the sense amplifier (SA) senses the ML voltage and gives the final match/miss decision. Fig. 1(b) shows the internal circuit of conventional NOR-type Ternary CAM (TCAM) cell which is less susceptible to failure due to the process variation as compared to NAND-type cell [7].

At the beginning of each search cycle, all MLs are pre-discharged to ground by the charging controller. During the evaluation stage, the search data register broadcasts the search data to the search-lines (SLs). If SL resembles stored bit D or the stored bit is X (don't care), the ML has no discharging path to ground and the path remains in the high-impedance state. If SL does not resemble D, the ML has a discharging path (through either transistors T_1-T_2 path or T_3-T_4 path) to ground. So, in a ML, the number of discharging paths is equal to the number of mismatches.

Fig. 2 shows the proposed charging controller. Here, at the beginning of search cycle, ML is pre-discharged to ground by a high MLP. The transistor M2 is turned ON by a low $\overline{\text{MLP}}$ and M5 is OFF by a low MLC; this causes M3 to be turned OFF. Therefore, charging of ML through M3 remains prohibited during the pre-discharging of ML.

During the evaluation stage, MLP is switched to low so

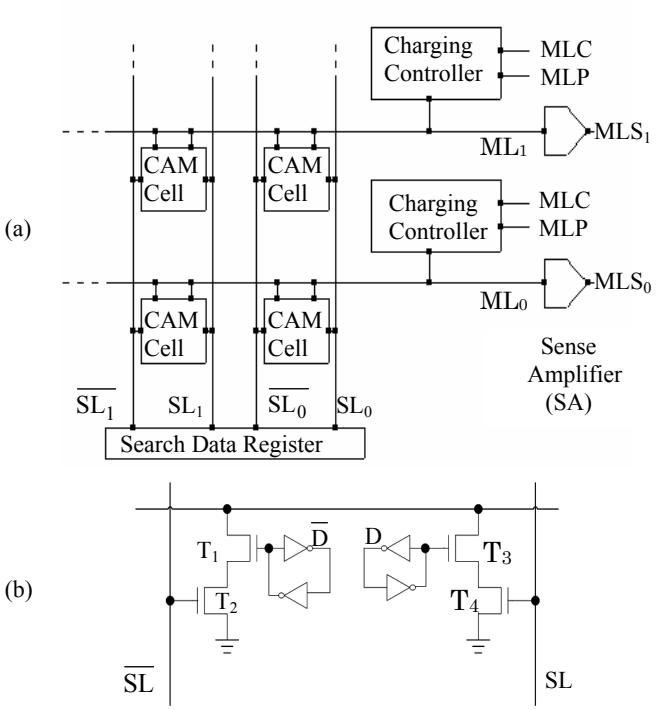

Fig. 1 Structure of the CAM of the proposed scheme: (a) basic architecture and (b) NOR-type TCAM cell used in the scheme.

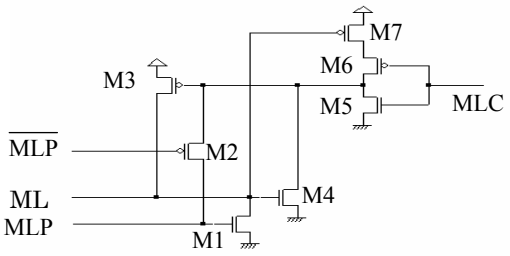

Fig. 2 Internal circuit of the charging controller.

that both M1 and M2 turn OFF. At the same time, MLC is switched to high so that charging of ML through M3 begins. If the CAM cell data of this ML is fully matched with the search-line data, then, there is no discharging path through the CAM cell. So, charging to the fully matched match-line (denoted by ML0) is faster than the partially matched match-line. MLC is kept high until the voltage of ML0 is enough to turn M4 ON; this causes the gate of the transistor M3 to be low and charging to ML0 continues via M3. As

the voltage of match-line, ML0 reaches about $V_{DD}/3$ and MLC is low, M6 becomes fully ON and M7 becomes partially ON. The end result is no more charging of ML through M3. The achieved voltage (~$V_{DD}/3$) of ML0 is high enough to be sensed as a high level for the proposed sense amplifier (SA). Now, the match-line which has one miss is denoted by ML1 and this ML is hardest to detect as a miss. As charging to ML1 is slower than ML0, the voltage of ML1 is not enough to be sensed as a high level by the SA.

Fig. 3 shows the proposed sense amplifier (SA). During precharge stage, the node SN is precharged to high through MS1. During the evaluation stage, when the voltage of ML is slightly above $V_{DD}/3$, the transistor MS2 turns ON. So, the node SN begins to discharge and MLS begins to rise. As MLS reaches high level, the transistor MS3 turns ON resulting in faster discharge of node SN. Transistor MS4 is used to initialize the output MLS to ground at the beginning of each search cycle.

3. Simulation Results and Analysis

The proposed scheme along with current-race and current-saving schemes are simulated using HSpice in the same 64 × 72 TCAM for TSMC 0.18µm CMOS process with the supply voltage of 1.8V.

Fig. 4 shows the simulation result for our design. At the beginning of a search cycle, MLP is high for 0.39 ns so that previously charged MLs can discharge to ground. Then, MLP is switched to low and MLC is switched to high for 0.33ns. As the voltage of ML0 rises up to 0.65V and MLC is low, the charging is stopped and the voltage of ML0 remains unchanged. The proposed sense amplifier senses this voltage as a match and output MLS0 turns to a full high level. On the other hand, the voltage of the ML1 rises up to 0.46V and then, degrades through the discharging path. The SA senses this voltage as a miss and results a low MLS1. As the difference between the maximum ML0 and ML1 (worst-case match-line) is 190 mV, even for a large process variation, our scheme will produce the correct search results.

Table I shows the comparative search energy and performance among the schemes. It shows that ML energy reduction is 57% and 54% compared to the current-race and current-saving schemes respectively and the speed is 3.13 times that of the both schemes.

The major difference between previous schemes [2]-[4] and our scheme is that we have used only one PMOS for charging the ML while previous schemes use two PMOS in series. So, the equivalent resistance is half of the previous schemes. Equivalent capacitance is also reduced. As a result, speed of the circuit increases. The basic difference between previous SA design [2]-[4] and the proposed SA is the switching threshold of SA. The proposed SA can sense a stable 0.6 V as a high level, whereas the previous SAs use ~1V as a switching voltage. So, the proposed scheme need not further charging after 0.6V (equals to $V_{DD}/3$) at ML0 is achieved. So, this scheme reduces a large amount of dynamic and leakage power, while a larger voltage swing of about $V_{DD}/2$ in [2]-[4] causes a higher power consumption.

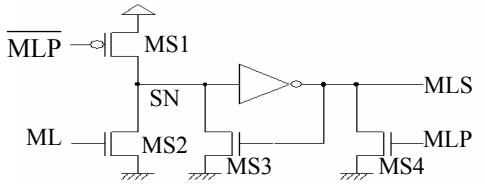

Fig. 3 Proposed sense amplifier (SA)

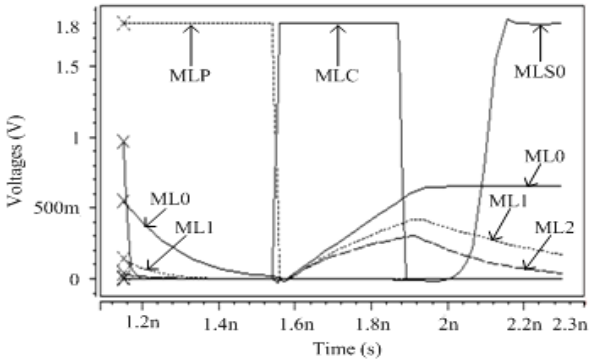

Fig. 4 Simulation results of the proposed CAM showing voltages ML0 (fully matched), ML1 (one-bit miss), ML2 (two-bit miss), MLC and MLP.

Table I Comparison of Different Schemes

Schemes	ML Energy (fJ/bit/ search)	SL Energy (fJ/bit/ search)	Minimum Cycle time, T (ns)	Speed, 1/T (MHz)
Current-race [2]	3.56	0.65	3.60	278
Current-saving [3],[4]	3.32	0.65	3.60	278
This work	1.53	0.62	1.15	870

4. Conclusion

This paper present a novel CAM scheme in which ML energy reduces by over 50% compared to previous current-race and current-saving schemes while the speed increases by over 3 times.

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