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Use of Current-Blocking Layer to Enhance Performance of Vertical GaN-Based Light-Emitting Diodes with a Ni-Plating Substrate

Kai-Ming Uang[1], Tron-Min Chen[1], Wei-Chi Lee[2], Pei-Ren Wang[2], Der-Ming Kuo[2], Yu-Yu Wang[2], Shui-Jinn Wang[2*], and Hon Kuan[3]

[1]Department of Electrical Engineering, WuFeng Institute of Technology, Chia-yi, Taiwan
[2]Institute of Microelectronics, Dept. of Electrical Eng., National Cheng Kung Univ., Tainan, Taiwan
[3]Department of Electro-Optical Engineering, Southern Taiwan University of Technology, Tainan, Taiwan
*Phone: +886-6-2757575-62351, Fax: +886-6-2763882, E-mail: sjwang@mail.ncku.edu.tw

1. Introduction

A great progress in display technology and solid-state lighting sources has been made by the use of GaN-based light-emitting diodes (LEDs) [1-2]. Above all, the improvement in efficiency and light power is important features for LEDs to promote the new era applications in photonics. Nevertheless, current spreading is still an imperative challenge for GaN-based LEDs due to *p*-GaN layer of relatively lower doping concentration and lateral-conducting structure using insulated sapphire. To alleviate the current crowding effect (CCE) and/or enhance the external quantum efficiency of conventionally lateral GaN-LEDs, efforts have been made by means of flip-chip technique [1], vertical conducting structure [3], or surface texturing [4], *etc.* Recently, the authors' group has developed Vertical-structure Metallic-substrate GaN-based Light-Emitting Diodes named as VM-LEDs [5-6], as shown in Fig. 1(a). Such an *n*-side-up vertical structure shows a significant alleviation for thermal and CCE of lateral LEDs. However, a substantial increase in efficiency must be achieved for competing with conventional lighting sources. Furthermore, a portion of injected carriers will be confined under the contact pad owing to its shortest current path. Accordingly, a considerable amount of generated light will be absorbed or reflected by the opaque metal pad. To solve this problem, a selective activation of p-GaN layer [7] or an insulating SiO_2 current blocking layer (CBL) [8] under the *p*-pad electrode was adopted for the lateral-conducting GaN-based LEDs. To further enhance the light output of regular VM-LEDs, we developed a CBL scheme for vertical GaN-based LEDs. In this work, the VM-LEDs with SiO_2 film as a CBL were fabricated by patterned LLO and Ni-plating technologies. The effectiveness of the CBL for vertical-structured GaN LEDs was also simulated and examined.

2. Experiments

The LED wafers used in this work were all grown on c-face 2 in. sapphire (0001) substrate by metalorganic chemical vapor deposition. The formation of CBL begins with the standard photolithographic patterning and inductively coupled plasma (ICP) etching process. To produce the CBL, the defined surface region (90 μm in diameter) of p-GaN layer was etched by ICP until the n-GaN layer was exposed. After that, an insulting SiO_2 layer as current blocking was formatted using plasma-enhanced chemical vapor deposition system and photolithographic process. To conduct the substrate transferring process, an oxidized Ni/Au layer was firstly deposited to serve as an Ohmic contact to *p*-GaN, followed by the deposition of a Ti/Al/Ti/Au multilayer as a reflective mirror/adhesive layer to the subsequent plated nickel layer. The electroplating process was then performed with a stable plating solution kept at about 55°C for 90 min.

The patterned LLO process was conducted using a KrF excimer laser (248 nm) directing through a quartz mask to the back of polished sapphire substrate. Device shape, dimension and space between two adjacent devices can be well defined by adjusting the spot size and the pitch between each two successive laser beam irradiations [5-6]. Surface of the separated GaN sample was then etched using ICP to remove the top *u*-GaN layer. Finally, a Cr/Al/Cr/Au layer was deposited on the cleaned *n*-GaN layer to serve as the *n*-type contact pad. Note that no thermal treatment was employed during the metallization process for the *n*-GaN. The schematic cross-section of fabricated *n*-side-up VM-LEDs with a CBL having electrodes on the top and bottom sides of the device is shown in Fig. 1(a). For comparison, regular VM-LEDs (without a CBL) as shown in Fig. 1(b) and conventionally lateral LEDs (with *p*-side-up lateral structure on sapphire substrate) with the same chip size of 300×300 μm^2, were also fabricated.

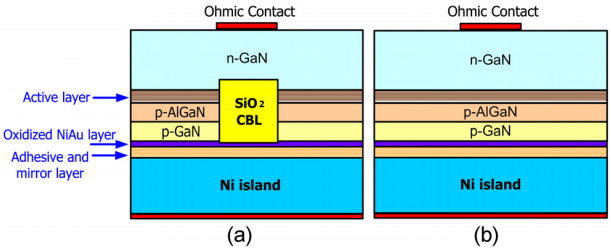

Fig. 1 Schematic cross-section of the fabricated device structures: (a) the VM-LED with CBL inserted in device structure and (b) a regular VM-LED.

3. Results and Discussion

The effectiveness of the proposed CBL schemes was verified by a two-dimensional device simulator (ISE-TCAD) and the calculated current density distributions across the active region of VM-LEDs were shown in Fig. 2. Note that the regular VM-LEDs have the largest current density underneath the n-contact pad. However, the CBL structure blocks and relieves the current crowding underneath n electrode and thus results in the reduction of photon absorption near cathode pad.

Comparison of measured I-V characteristics of fabricated LEDs is shown in Fig. 3. It reveals that the typical forward voltage drop (V_f) of conventional LEDs, regular VM-LEDs, and VM-LEDs with a CBL at 20 mA is about 3.41, 3.03, and 3.14 V, respectively. As compared to conventional LEDs, the reduction in V_f of the VM-LEDs is mainly attributed to the use of a metallic substrate, enabling a relatively less current crowding effect as well as a shorter and higher conductivity of the current conduction path. Note that the use of CBL causes just a slight increase (~0.11 V) in V_f of fabricated VM-LEDs, still favoring the

high-current operations. Figure 4 illustrates the comparison of electroluminescence (EL) spectrum obtained from conventional LEDs and VM-LEDs with and without a CBL at room temperature. The inset of the figure demonstrates photo of light emission at 20 mA from the VM-LED with a CBL. The EL spectrum of the VM-LED shows the peak wavelength (λ_p) located around 458.1 nm without multipeaked emission, under an injection current of 20 mA. It is evident that, as compared to conventional LEDs, a considerable improvement in EL intensity of VM-LEDs was achieved. Note that the EL intensity of VM-LEDs was further enhanced as a result of the insertion of insulated CBL. Such an improvement should be ascribed to the reduced current crowding under opaque metal n-pad.

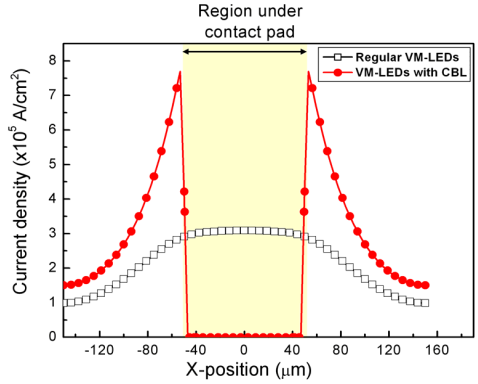

Fig. 2 Calculated current density distribution across the active region of the VM-LEDs with and without a CBL.

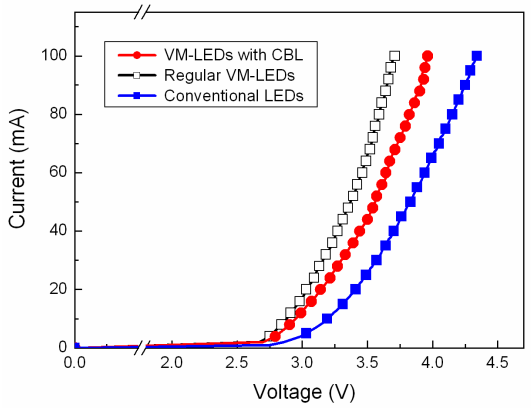

Fig. 3 Comparisons of measured I-V characteristics of conventionally lateral LEDs and VM-LEDs with and without a CBL.

Figure 5 shows the measured light output power–current (Lop-I) characteristics of VM-LEDs without and with SiO_2 CBL. The measured Lop-I curve of a conventional LED is also shown. An improvement in Lop of the regular VM-LED was about 80% at 20 mA as compared to that of the conventional LED, while for the VM-LED with a SiO_2 CBL, an increase in Lop as high as 143.6% was achieved. In addition, the Lop of the VM-LED chip with an insulating SiO_2 CBL at 20 mA was typically increased by 35.4% compared to that of the one without CBL, although the light-emitting area was reduced due to the insertion of CBL structure. In essential, as compared to the conventional LED, the VM-LED offers not only a much better capability of current spreading but also a relatively larger light-emitting area. Note that the use of SiO_2 CBL can further enhance the Lop of VM-LEDs, even though the optimization of CBL structure is under way. Such an enhancement in Lop of VM-LEDs could be again attributed to effectiveness of an inserted CBL in increasing current injection into the active layer except for the region beneath opaque metal pad and reducing optical absorption at n-contact pad.

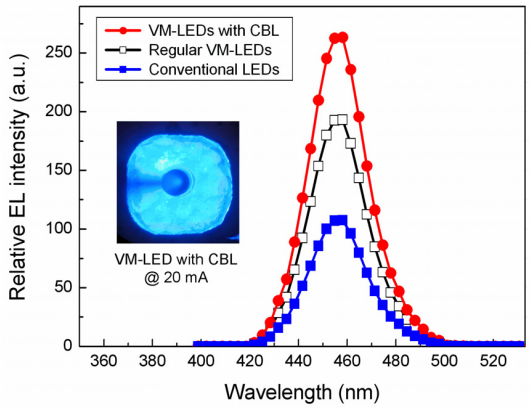

Fig. 4 EL spectrum obtained from various LED structures. The inset shows photo of light emission from VM-LEDs with a CBL at 20 mA.

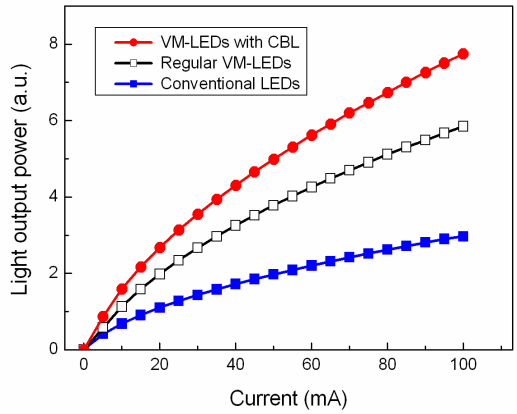

Fig. 5 Comparisons of measured Lop-I characteristics of various LED structures.

4. Conclusions

In summary, the fabrication and characterization of vertical GaN-based LEDs having a SiO_2 CBL under the n-pad has been demonstrated. With the insertion of CBL into the VM-LED structure, an improvement in light output power by 35.4% at 20 mA was achieved, as compared to that for the vertical LED chip without CBL. It is expected that the use of optimal structure for SiO_2 CBL would make possible the fabrication of VM-LEDs with even higher power and better efficiency.

Acknowledgments

This work was supported in part by National Science Council of Taiwan, R. O. C., under Contract Nos. NSC 96-2221-E-006-081-MY2, NSC 96-2221-E-274-011, and the Landmark Project Grant for NCKU's Top-University Project.

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