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CMOS Paradigm Change through Material Integration on a Chip

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1. Introduction

The device scaling concept had long been the guiding principle for designing MOSFETs, while it had often faced with difficult challenges. The barriers had been overcome by a considerable amount of technological innovations such as poly-Si gate self-aligned MOSFET (1966), ion-implanted channel (1969), lightly doped drain (1980), self-aligned silicide (1981), Halo doping (1985), shallow trench isolation (1988), CMP (1989), strained Si channel (1992), Cu interconnect (1993), etc. [1]. Most of these technologies have been systematically implemented in state-of-the-art CMOS platform. Now under the sub-50nm regime, MOSFET performance enhancement and the variation control must be achieved through the tradeoff among on-current, power dissipation primarily due to off-current and its variation under short channel effects. Introducing new device architectures and new materials will significantly extend the physical parameter space for CMOS design [2, 3]. This implies that CMOS is stepping into a new paradigm at the device level and certainly at the circuit level as well. This paper reviews recent achievements of the MIRAI Project on science and technology of rapidly evolving CMOS devices and multilevel interconnects, and tries to get physical insights in the future direction of devices and materials research.

2. Carrier - Transport - Enhanced CMOS

While the mobility in MOSFETs is still an important parameter to describe the current drive, the reduction in the effective mass is more essential in the increase of the on-current under full-ballistic or quasi-ballistic regime although the inversion layer capacitance is degraded with lower effective masses [4, 5]. For further extending such concepts to future device technology, we need to realize (1) continued enhancement of carrier transport properties based on new materials, (2) optimal design of nMOS and pMOS channel architectures and materials, and (3) compatibility with multi-gate structures or exotic non-planar channels.

2.1 Biaxially Strained Planar CMOS

One possible way to dramatically enhance hole transport properties is to employ a pure Ge or high-Ge-content SiGe on insulator (GOI or SGOI) with biaxial compressive strain for pMOSFET channels. Hole mobility enhancement of 10x compared to the Si hole mobility has been achieved, in which 5x is due to a high Ge content (93%) and 2x due to remaining compressive strain (1.5%) [6]. As for nMOSFET, biaxial tensile strain induces 1.6-2.0x electron mobility enhancement. Integration of such strained-SOI nMOSFET and strained-SGOI pMOSFET on the single SGOI wafer has been demonstrated by using local Ge condensation of the SiGe layer and selective epitaxy of strained-Si layer on SiGe [7].

2.2 Uniaxially Strained Multi-gate CMOS

The uniaxial strain configuration is well suited for multi-gate structures such as FinFETs and Tri-gate MOSFETs, because such 3D device structures enable to simultaneously combine three independent mobility enhancement mechanisms, namely, (110) surface orientation, uniaxial compressive strain, and SGOI channel. Indeed a Tri-gate SGOI pMOSFET with the (110) sidewall channels with uniaxial compressive strain along the <110> current flow direction has shown the Gm enhancement of 3x with respect to that of planar Si(100) MOSFET [8]. Such uniaxial strain configuration is also applicable to n-channel FinFETs by using strained SOI (SSOI) as a starting substrate. The Si (110) surface electron mobility is much lower than that on (100), and thus the performance of unstrained n-channel FinFETs along <110> is problematic. The uniaxial tensile stress along <110> induces the electron transfer from the 4-fold valleys with the higher effective mass to the 2-fold with the lower mass which leads to the mobility increase [9, 10]. It has been shown that uniaxially tensile-strained SSOI Tri-gate FETs realize 2.2x of the Gm compared to conventional SOI Tri-gate FET, indicating the effectiveness of the subband engineering [9]. Those results show that the optimal design of multi-gate CMOS architecture under uniaxial strain can be realized by combining tensile-strained SSOI nMOSFET and compressively strained SGOI pMOSFET along the same <110> current flow direction.

3. Metal/High-k Gate Stack

It is a central problem of high-k CMOS technology that V_{TH} of high-k MOSFETs cannot be designed with a conventional way as is known for SiO_2 MOSFETs. The anomalous V_{FB} shift in poly-Si gate CMOS has been pointed out by Hobbs et al. and explained by the Fermi-level pinning (FLP) model [11].

3.1 Mechanism of V_{FB} Anomaly and V_{TH} Control

Recently it has been found that the dipole layer at the HfLaOx/SiO_2 interface plays a predominant role in the V_{FB} shift which is in proportion to the La concentration. It is also shown that the dipole layer is localized at the insulator (high-k)/insulator (SiO_2) heterointerface [12]. To obtain the further insight in the dipole layer formation mechanism, stacked bi-layer high-k dielectrics have been grown by the ALD technique. It has been demonstrated that the dipole moment strength located at the bottom-layer high-k/SiO_2 interface changes exponentially with the high-k thickness within a scale of one or two monolayers. Furthermore, it has been shown that the interface dipole direction of Al_2O_3/SiO_2 and HfO_2/SiO_2 is opposite to that of La_2O_3/SiO_2 [13]. This

bottom layer dipole can quantitatively explain most of V_{FB} anomalies ever reported on the metal/high-k/SiO_2/Si systems.

By considering the strength and direction of the dipole moment in the high-k/SiO_2 interface, the V_{TH} values for n- and p-MOSFET could in principle be adjusted with a single metal gate.

3.2 Inversion Layer Mobility: Scattering Mechanism

The inversion layer mobility of high-k MOSFETs has been more or less deteriorated as compared to the SiO_2 MOSFET mobility particularly in the thinner EOT (equivalent oxide thickness) regime. The mobility degradation could be caused by the remote phonon scattering (RPS) [14]. In order to reveal the influence of the RPS, the electron mobilities for MOSFETs with HfO_2 gate dielectrics having different crystalline phases, monoclinic and tetragonal, which exhibit distinctly different IR-active optical phonon spectra, have been comparatively studied. The measured mobilities including the temperature dependence for tetragonal and monoclinic HfO_2/SiO_2 stacks, however, are quantitatively very similar. It is also found that the extent of mobility degradation and the magnitude of the interface dipole moment as defined by ΔV_{FB} are well correlated. This also indicates that the carrier scattering due to the dipole layer at the HfO_2/SiO_2 interface reduces the high-k FET mobility [15].

3.3 Scalability of High-k Gate Stack

For aggressive EOT scaling, the interfacial layer (IL) should be thinner and higher-k than the case of SiO_2. It has experimentally been shown that uniform silicate formation reaction between Si and sub-monolayer ALD-grown HfO_2 appears to proceed more efficiently than Si oxidation [16]. By using this silicate layer as IL, 0.5nm EOT MOSFET operation has been demonstrated [17]. Further EOT scaling might be possible if cubic phase HfO_2 with a very high-k value of ~50 can be used for the gate stack [18].

4. Ultra Low-k/Cu Interconnects

A straightforward way to realize ultralow dielectric constant is to introduce nanoscale pores into dielectrics such as silica-based materials. However, increasing the porosity is accompanied with considerable deterioration of the mechanical strength or Young's modulus of low-k films and moisture adsorption on the pore wall surfaces. To solve this dilemma an innovative process, silylation hardening, has been proposed and successfully applied to high-porosity silica films [19].

4.1 Silylation Hardening of Porous Silica Films for Scalable Cu Damascene Multilevel Interconnects

Porous silica films were formed by use of self-assembly of surfactant and silica oligomer. The pore diameter was controlled by changing the surfactant molecular weight as confirmed by ellipsometric porosimetry. Spin-coated films were UV-cured at 350°C, followed by silylation hardening process with TMCTS (Tetramethylcyclotetrasiloxane) vapor anneal at 350°C [20, 21]. Thus produced silica films have a high porosity (50%), an ultra low-k (k=2.1) and a high modulus (E>9GPa), being applicable to interlayer dielectrics [22].

The mechanical strength of ultra low-k porous silica film is basically determined by defects existing in the pore wall. Those defects can be passivated by TMCTS vapor anneal (silylation treatment), and thus the polymerized TMCTS monolayer formation on the pore wall surface reinforces the skeletal silica network (silylation hardening) and consequently the pore wall surfaces become hydrophobic.

32-nm node ultralow-k (k=2.1) self-assembled porous silica/Cu damascene multilevel interconnects have been fabricated. It is demonstrated that the interlayer dielectric patterning with silylation treatment for etch damage recovery and subsequent CVD-SiC sidewall film deposition for managing the interline leakage current are key steps to achieve the 32-nm node multilevel interconnects and beyond [22].

Summary

New device architectures and new materials introduced to the Si-based CMOS platform will open up a pathway to obtain the required performance particularly when special efforts are paid to establish scientific knowledge basis on new concept devices and interconnects.

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References

[1] H.-S.P. Wong, VLSI Devices, ed. by C.Y. Chang and S.M. Sze (Wiley, NY, 2000) Chapter 3.
[2] S. Takagi et al., IEEE Trans. Electron Devices, 55 (2008) 21.
[3] A. Toriumi et al., IEDM (2007) 53.
[4] K. Natori, J. Appl. Phys. 76 (1994) 4879.
[5] M. Lundstrom and Z. Reu, IEEE Trans. Electron Devices, 49 (2002) 133.
[6] T. Tezuka et al., VLSI Symp. (2005) 80.
[7] T. Tezuka et al., Semicond. Sci. Technol. 22 (2007) S93.
[8] T. Irisawa et al., IEDM (2005) 727.
[9] T. Irisawa et.al., IEDM (2006) 457.
[10] K. Uchida et al., IEDM (2005) 135.
[11] C-C. Hobbs et al., VLSI Symp. (2003) 9.
[12] Y. Yamamoto et al., Ext. Abst. SSDM (2006) p. 212.
[13] K. Iwamoto et al., VLSI Symp. (2007) 70.
[14] M.V. Fischetti et al., J. Appl. Phys. 90 (2001) 4587.
[15] H. Ota et al., IEDM (2007) 65.
[16] A. Ogawa et el., Microelec. Engn. 84 (2007) 18651.
[17] M. Takahashi et al., IEDM (2007) 523.
[18] S. Migita et al., VLSI Symp. (2008) 152.
[19] T. Kikkawa et al., IEDM (2005) 99.
[20] K. Kohmura et al., Mat. Res. Soc. Symp. Proc. Vol. 812 (2004) F6.2.
[21] R. Yagi et al., VLSI Symp. (2005) 146.
[22] S. Chikaki et al., IEDM (2007) 969.