Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp8-9

A-1-1(Invited)

Ultrathin Body and BOX SOI and sSOI for Low Power Application at the 22nm technology node and below

F. Andrieu, C. Fenouillet-Béranger*, O. Weber, S. Baudot, C. Buj, J.-P. Noel, O. Thomas, O. Rozeau, P. Perreau*, L. Tosti, L. Brévard, O. Faynot

CEA LETI, Minatec, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France
Phone: +33-4-3878-2752 E-mail: francois.andrieu@cea.fr
*also with STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France

1. Introduction

Advanced CMOSFETs technologies on bulk are facing the major challenge of the variability. Indeed, from node to node, the channel doping has historically increased in order to maintain a good electrostatic control, ensuring the technology scaling. However, this trend degrades the Random Dopant Fluctuation, which limits the ultimate working margin of SRAMs. Design solutions currently tend to overcome this variability issue, but with some area penalties. The device solution of this problem would consist of thin undoped channel MOSFETs, where the electrostatics is governed by the film thickness whereas the low channel doping enables a high immunity against variability.

The FDSOI device integration requires technological modules: especially raised source/drain in order to minimize the parasitic access resistance [1] and a metal gate in order to adjust the threshold voltage [2]. Fortunately, these two breakthroughs were respectively used by IC's manufacturers since the 90nm and 45nm nodes respectively on bulk CMOSFETs [3]. This open up both a technical and psychological window for the integration of Fully Depleted Silicon-On-Insulator devices for the 22nm node and below.

In this abstract will be reviewed the FDSOI technology in terms of performance, multi-threshold voltage (V_T) options and SRAM.

2. Performance

The Ion-Ioff tradeoff of n- and pMOSFETs integrated at V_{DD}=1V with an HfO_2/TiN gate stack on 10nm thin body FDSOI are summarized in Fig.1. Note that the Equivalent Oxide Thickness was 1.65nm in these experiments. Nevertheless, the overall performance is rather good, mainly for narrow channel devices. In order to understand this behavior, we carried out some Grazing Incident X-Ray Diffraction at the European Synchrotron Radiation Facility (ESRF, Grenoble, France) on mesa-isolated SOI surrounded by the gate stack. It highlighted the strong influence of the TiN gate that induces a tensile strain, reaching more than 0.5% for 50nm wide SOI lines. Based on the piezo-resistive coefficients, such a type of strain (tensile and perpendicular to the transport direction) is beneficial for nMOS and even more for pMOS [4]. This is probably one explanation of the huge boost of performance in narrow devices (especially pMOS) integrated without intentional stressors (Fig.1).

Contact Etch Stop Layers (CESLs) have been used in order to improve further the short channel carrier velocity. They enable an up to 20% (90%) Ion improvement for narrow pMOS (respectively nMOS). This can be directly correlated with short channel mobility boost, which is also greater in narrow transistors [4]. Finally, 1000µA/µm for nMOS and 550µA/µm Ion at Ioff=100nA/µm are reached with FDSOI and CESLs. This performance is obtained thanks to very good access resistance, around 200Ohm.µm, (value confirmed by different methods [5-7]).

Note that the Ion can be further boosted by a strained SOI (sSOI) substrate for nMOS (Fig.1) and, most of all, by an EOT shrink for both n&pMOS. On the other hand, to reduce the Ioff in the future, we demonstrated that thinning the Si body is the first effective solution [6].

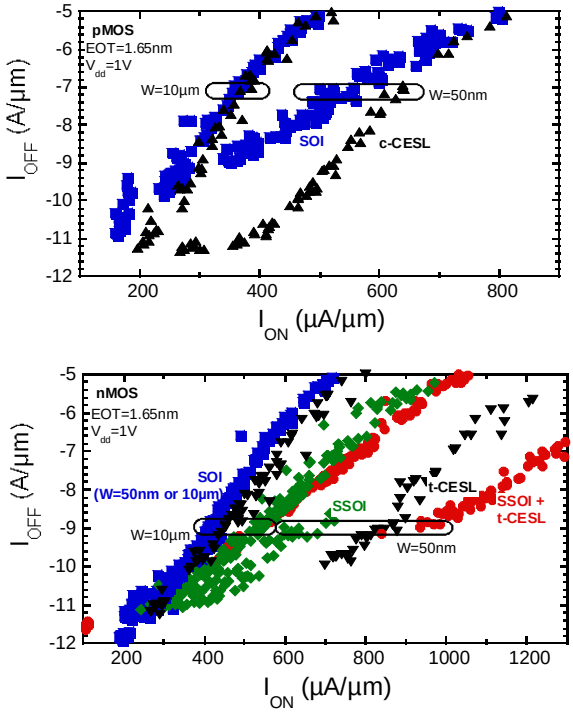


Fig. 1 Ion-Ioff trade-offs for pMOS (top) and nMOS (bottom) (along the <110> channel direction) with a mesa isolation and different stressors at V_{DD}=1V for wide (W=10µm) and narrow (W=50nm) (top-view normalisation).

RF measurements were also carried out on unstrained FDSOI nMOS. These transistors yields f_T=118GHz at L_G=70nm [7]. It must be pointed out that the threshold voltage of the tested nMOS is above 0.4V and thus non-optimized for high speed applications. In order to benchmark this value with the literature ones, we plotted the f_T vs. the Ion/Ioff ratio (Fig.2). We can see that the tested devices offer very good compromise: clearly target-

ing Low STandby Power applications and demonstrating a promising f_T>100GHz, at the same time.

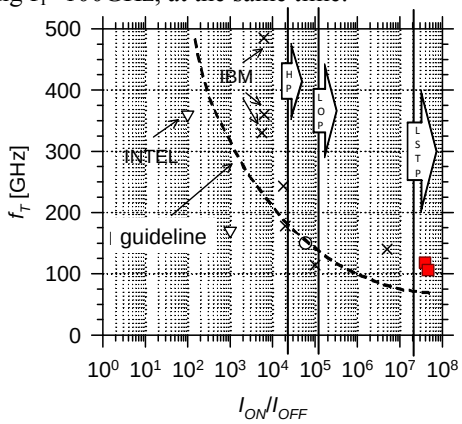


Fig. 2 f_T vs. Ion/Ioff ratio for a nMOS at L_G=70nm (red squares), compared w/ literature results [7].

3. Multi-V_T options

The threshold voltage (V_T) tuning on bulk Si with metal gates is a big challenge; mainly for pMOS because it requires p+ workfunction. On the contrary, the V_T adjustment on FDSOI with an undoped channel only requires gate workfunctions around the midgap (see the yellow diamond in Fig.2). In particular, 2 metal gates at 0.15eV from the mid-gap yield 2 V_{Ts} (LVT and HVT) for both n- and pMOS. An extra tuning of V_{Ts} is possible with a channel doping without a too severe degradation of performance ([8] and circle on Fig.3).

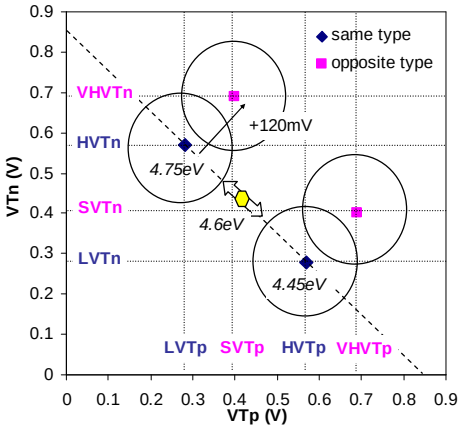


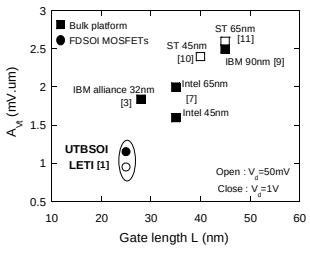
Fig. 3 Different threshold voltages available for nMOS (VTn) and pMOS (V_{Tp}) on FDSOI with only two gates (whose worhfunction is 4.45eV and 4.75eV) i) on thick BOX or UTBOX w/o any ground plane doping or w/ one of the same type as the source/drain (n type for nMOS and p type for pMOS) (blue diamonds) or ii) on UTBOX w/ a ground plane doping of the opposite type (pink squares). The circles correspond to the V_T sensibility to a ±0.9V back-bias polarisation on UTBOX or to a channel doping around 2 10^{18}cm^{-3}.

The other solution to adjust V_T in FDSOI is to use Ultra Thin Buried OXide substrates (UTBOX) and a ground plane doping, which i) provide 2 additional V_{Ts} (Very High and Standard VT) or more if a back-bias is used [13] and ii) enable power management thanks to back-biasing (around 120mV/0.9V sensibility) ([9] and Fig.3).

4. SRAM

One of the first 32nm SRAM cell (0.179µm^2) demonstration was done in FDSOI [10], proving that this technology can be ultra-compact. In the future, the trade-off between the density and the minimum voltage at which SRAM arrays are functional (V_{min}) could be improved further thanks to the FDSOI technology and its record A_{Vt}, as highlighted in Fig.4 and [11-12]. This is directly induced by the undoped channels (decreasing the Random Dopant Fluctuations) and the exceptional electrostatic control of this technology.

UTBOX substrates enable pursuing this electrostatics improvement (especially DIBL and short channel subthreshold slope) [9]. Furthermore, they allow a double-gate like control of the channel thanks to the back-bias contact. This flexibility is illustrated in Fig.5 by an original SRAM design possible thanks to UTBOX with an excellent theoretical performance and a high manufacturability [13].



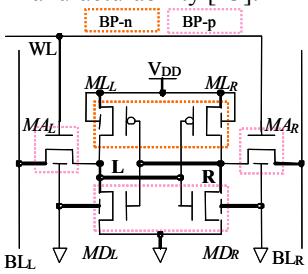


Fig. 4 (left) Summary of the bulk literature results. A_{Vt} is defined as $\sigma_{VT}=A_{VT}/(W.L)^{0.5}$. From $\sigma_{\Delta VT}$ obtained on pairs FETs, the formula $\sigma_{VT} = \sigma_{\Delta VT}/\sqrt{2}$ is used.
Fig.5 (right) Schematic view of a HVT 6T SRAM cell in UTBOX FDSOI technology with ground plane and back-biasing.

5. Conclusion

The FDSOI technology already demonstrated its performance (especially thanks to the compatibility with some stressors), its scalability (thanks to a body thickness and/or BOX reduction) and its design friendliness (with multi-V_T availability and design proximity with bulk if UTBOX substrates are used).

Acknowledgements

This work has been carried out in the frame of the LETI / ST Microelectronics joint program, the OSEO Nanosmart project and the Medea+ DECISIF, in collaboration with SOITEC.

References

[1] R. Chau et al., IEDM Tech. Dig., p. 621-3, 2001. [2] H. Shimada et al., IEEE TED, p. 1903-7, 1979. [3] C. H. Jan et al., IEDM Tech. Dig., p. 1-4, 2008. [4] S. Baudot et al., to be presented at ESSDERC, 2009. [5] F. Andrieu et al., SSDM, pp. 888-9, 2007. [6] V. Barral et al., IEDM Tech. Dig., p. 61-4, 2007. [7] T. C. Lim, SSE, 53, p. 433-7, 2009. [8] C. Buj et al., to be presented at SSDM, 2009. [9] C. Fenouillet et al., to be presented at ESSDERC, 2009. [10] C. Fenouillet et al., IEDM Tech. Dig., p. 267-9, 2007. [11] K. Itoh et al., ESSDERC, p. 68-75, 2007. [12] O. Weber et al., IEDM Tech. Dig., p. 245-8, 2008. [13] J. P. Noel et al., to be presented at ESSDERC, 2009.