Abstract

$V_{th}$ variations by random dopant fluctuations (RDF) in intrinsic channel SOI MOSFETs with ultra-thin BOX are investigated by 3D device simulation. It is found that, contrary to bulk and doped channel SOI MOSFETs, $V_{th}$ variations in intrinsic channel SOI MOSFETs decrease with increasing $V_{th}$. The device design guideline for intrinsic channel SOI MOSFETs is also discussed.

1. Introduction

Increasing variability of $V_{th}$ is a critical issue for further device scaling. In current bulk MOSFETs, one of the major sources of $V_{th}$ variability is RDF [1,2]. In particular, bulk MOSFETs with high $V_{th}$ severely suffer from $V_{th}$ variability due to high impurity concentration in channel region. Therefore, a FD SOI MOSFET and a FinFET, using an intrinsic channel to eliminate RDF and controlling $V_{th}$ by gate workfunction engineering, have been proposed. Despite of many substantial advantages in these devices, they have not adopted for mass production yet. One of the reasons is that the process for multiple-workfunction-metal-gate-electrode is very difficult.

On the other hand, it has been found that an intrinsic channel FD SOI structure with ultra-thin BOX and a high impurity concentration substrate is effective not only in reducing RDF but also in controlling $V_{th}$ by changing substrate impurity concentration [3-5] without applying back bias voltage. Therefore, this device is promising for multiple-workfunction-electrode devices applications. However, $V_{th}$ variations in different $V_{th}$ in the intrinsic channel FD SOI have not been cleared yet.

In this paper, we investigate the $V_{th}$ dependence of $V_{th}$ variability in the intrinsic channel FD SOI MOSFETs with ultra-thin BOX. Extremely small $V_{th}$ variations due to RDF compared with bulk and doped SOI is demonstrated and its physical understanding is discussed.

2. Simulations

Fig.1 shows schematics of the intrinsic FD SOI with ultra-thin BOX, bulk MOSFETs, and doped channel SOI assumed in this paper. A midgap metal gate electrode is assumed, $L_g$ and $W_g$ are 40nm, $t_{ox}$ is 1.2 nm, and $V_a$ is 1.0V. In SOI MOSFETs, 5-nm and 10-nm BOX layer are assumed, and SOI thickness is 10 nm. The impurity concentration of substrate ($N_{SUB}$) is changed in the intrinsic channel SOI, and the channel concentration ($N_A$) is changed in doped SOI and bulk MOSFETs. By the Monte-Carlo 3D device simulation assuming random dopant distribution, $V_{th}$ of 200 samples is calculated for each condition and the standard deviation of $V_{th}$ ($\sigma V_{th}$) due to RDF is derived.

3. Results

3.1. Characteristics of intrinsic channel SOI MOSFET:

Fig. 2 shows simulated $I_d-V_{th}$ characteristics of an intrinsic FD SOI MOSFET with thin BOX. No considerable degradation of subthreshold slope (SS) due to short channel effect (SCE) is observed even at very low $N_{SUB}$. Fig. 3 shows $V_{th}$ as a function of $N_{SUB}$. $V_{th}$ increases as $N_{SUB}$ increases. However, at high $N_{SUB}$, $V_{th}$ saturates and increases only very slightly. This saturation, which is clearer at thicker $t_{BOX}$, leads to smaller $\sigma V_{th}$ as mentioned later.

Fig. 4 shows the depth profile of the potential in long channel SOI MOSFETs. At high $N_{SUB}$, the potential at the interface between BOX and substrate sticks to high level due to extremely thin depletion layer, and this causes the $V_{th}$ saturation. Figs. 5 and 6 show $V_{th}$ as a function of $t_{BOX}$ at $L_g$ of 40nm and 1um, respectively. $V_{th}$ increases monotonically as BOX becomes thinner in long channel, while $V_{th}$ decreases in short channel only when $N_{SUB}$ is low. This decrease in $V_{th}$ is caused by the fringing field through BOX and substrate induced by drain voltage [6].

3.2. $V_{th}$ variations of intrinsic channel SOI MOSFET:

Fig. 7 shows simulated $\sigma V_{th}$ as a function of $N_{SUB}$. Data in bulk and doped SOI MOSFETs are also shown. In the bulk and doped SOI MOSFETs, $\sigma V_{th}$ rapidly increases as $N_{SUB}$ increases, which is typical and unavoidable in conventional devices. However, in the intrinsic channel SOI MOSFETs, extremely high RDF immunity is clearly observed. Moreover, $\sigma V_{th}$ decreases as $N_{SUB}$ increases, which is never observed in conventional devices. The increase in $\sigma V_{th}$ at low $N_{SUB}$ is caused by the $V_{th}$ decrease by the fringing field mentioned above.

Fig. 8 shows simulated $\sigma V_{th}$ as a function of $V_{th}$. It is confirmed that the intrinsic channel SOI MOSFET has much smaller $\sigma V_{th}$ at a given $V_{th}$, and that $\sigma V_{th}$ decreases as increasing $V_{th}$. The result indicates this device is very suitable for low power devices with high $V_{th}$. It is also found that, although a device with thinner $t_{OX}$ (5nm) has larger $\sigma V_{th}$, it can control $V_{th}$ in a wider range. Fig. 9 shows the cumulative probability plot of $V_{th}$ in the intrinsic channel SOI MOSFET, which shows Gaussian distributions.

Based on these results, we can derive a practical design guideline of intrinsic channel FD SOI MOSFETs with ultra-thin BOX. There exists a tradeoff between $\sigma V_{th}$ and $V_{th}$ control range. By adjusting $t_{BOX}$ and choosing high $N_{SUB}$, $V_{th}$ can be controlled while maintaining $\sigma V_{th}$ very small.
4. Conclusions

Extremely high RDF immunity and good $V_{th}$ controllability in FD SOI MOSFETs with thin BOX and highly doped substrate was demonstrated. It is confirmed that the device has very small $\sigma V_{th}$ even at high $V_{th}$, indicating the device is very suitable for a low power device.

**Fig.1** Schematic views of (a) intrinsic channel FD SOI with ultra-thin BOX, (b) bulk, and (c) doped channel SOI MOSFETs.

**Fig.2** $I_d-V_g$ characteristics with different $N_{SUB}$ in intrinsic channel SOI MOSFET. No considerable degradation of $SS$ is observed.

**Fig.3** $V_{th}$ dependence of $V_{th}$ in short channel intrinsic channel SOI MOSFET. At high $N_{SUB}$, $V_{th}$ saturates.

**Fig.4** Simulated potential depth profile. At high $N_{SUB}$, the potential at interface between BOX and substrate sticks to high level due to extremely thin depletion layer.

**Fig.5** $t_{BOX}$ dependence of $V_{th}$ in short channel intrinsic channel SOI MOSFET.

**Fig.6** $t_{BOX}$ dependence of $V_{th}$ in long channel intrinsic channel SOI MOSFET.

**Fig.7** Simulated $\sigma V_{th}$ as a function of $N$. In bulk and doped channel SOI, $N$ is equal to $N_A$. In intrinsic channel SOI, $N$ is equal to $N_{SUB}$.

**Fig.8** Simulated $\sigma V_{th}$ as a function of $V_{th}$. A high $\sigma V_{th}$ in bulk at low $V_{th}$ is caused by SCE.

**Fig.9** Cumulative probability plot of $V_{th}$ in intrinsic channel SOI MOSFETs.

**Reference**


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