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Counter-doping as a solution for multi threshold voltage on FDSOI MOSFETs with a single TiN/HfO_2 gate stack

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ABSTRACT

We evidence the advantages and drawbacks of counter doping as a solution to locally lower the threshold voltage of 10nm thin FDSOI n and pMOSFETs integrated with a single TiN/HfO2 gate stack. Thanks to the counter doping, a 100mV Vth decrease is typically obtained per 5E12 at/cm2 implanted species on long channel as well as short channel MOSFET, without significant degradation of the performance and the electrostatic behavior.

INTRODUCTION

With CMOS scaling down, thin film devices become more and more attractive because of their excellent short channel control [1]. Moreover, integrated with a single midgap metal gate (such as TiN) on a high-k dielectrics, undoped FDSOI devices present a long channel V_{th} around ±0.45V for n and pMOS [3]. For these two reasons, they are of great interest for ultra-low power applications.

However, a smaller V_{th} is required for analog or RF applications. In order to achieve such a V_{th} (around 0.2-0.3V), a counter doping implantation into the channel region seems to be an effective and attractive technique. In this work, we thus discus the advantages and drawbacks of accumulation mode FDSOI MOSFETs in terms of process integration, V_{th} tuning, logic and analog performances and variability.

PROCESS DESCRIPTION

Standard SOI substrates (with 145nm buried oxide) have been used for this analysis. The top silicon thickness has been thinned down to T_{si}=10nm using sacrificial oxidations. After active area patterning and etching (MESA isolation), Arsenic and BF_2 implantations have been used to dope the channel of the n and pMOS transistors, respectively (see figs 1a &1b). The implantations conditions have been defined by process and electrical simulations (see Fig. 1).

The gate stack has then been deposited (3nm ALD HfO_2 + 10nm PVD TiN + 50nm n+ doped poly-silicon). After the gate etching, a 10nm thick nitride spacer has been fabricated prior the HfO_2 etch. A 2-step selective epitaxy process has been done in order to reduce the access resistance [3]. NiSi has then been used, followed by a standard BEOL process. Fig. 2 shows a TEM image of the device.

ELECTRICAL RESULTS AND DISCUSSION

Fig. 3 presents the threshold voltage roll-off curves at V_{DD}=1V for n and pMOS and for the various counter-doping conditions. A V_{th} reduction for long as well as for short channels is achieved thanks to the counter doping. Note that the variation of threshold voltage is kept quasi independently of the gate length. Fig. 4 confirms it, summarising this V_{th} variation of the threshold voltage obtained for different implanted doses. For both n and pMOSFETs, a 100mV V_{th} decrease is obtained per 5 10^{12} at/cm^2 implanted species in the channel. This demonstrates the efficiency of the channel doping, even on FDSOI devices, in order to tune the threshold voltage.

The classical drawback of the counter-doping is the degradation of the electrostatic control. However, there are few (no? XXX) experimental data of the influence of the counter-doping on 10nm thin FDSOI MOSFETs. Fig. 5 shows the DIBL evolution as a function of the implanted dose. The DIBL is slightly degraded in the accumulation-mode regime. For intrinsic nMOS devices at the nominal gate length (35nm), the DIBL is around 100mV and goes up to 120mV for 10^{13} cm^{-2} implanted dose (corresponding to a -200mV V_{th} lowering). The same behaviour is observed for the pMOS. The DIBL is around 120mV for the intrinsic PMOS devices and goes up to 150mV for 5 10^{12} implanted dose (corresponding to a 100mV V_{th} lowering). This degradation seems however acceptable for some applications, in RF devices, for example.

The subthreshold swings of short nMOSFETs are not degraded with the counter-doping (Fig.5). In particular, excellent values of 80mV/decade are always measured on short nMOS devices, whatever the counter-doping conditions. For pMOS devices, 90mV/decade is measured for doped channels, while 80mV/decade is measured on intrinsic ones.

I_{ON}(I_{OFF}) data for n and pMOS transistors are shown on Figs. 6&7, respectively. As, expected, the counter-doping increases the leakage current in long channel devices because of the threshold voltage lowering. This V_T shift is the main reason for the different shape of the I_{ON}-I_{OFF} with different channel dopant concentrations. This is clearer when you compare the performance at a given gate length (I_{OFF} shift rather than an I_{ON} shift evidenced in Figs 6&7). Only a 4% I_{ON} degradation (per 5E12 at/cm2 implanted species) of the drive current trade-off is observed at a given I_{OFF}=100nA/µm. Note that in this comparison at a given I_{OFF} is not easy to interpret because, in this case, the effective electric field and the gate length are not the same in the doped and undoped channel.

In order to get more data about the electron or hole transport in these devices, the maximum of transconductance ($G_{M,max}$) at VD=50mV for short channel MOS (fig 10) and the mobility for long channel MOS, were measured [4] (Figs. 8&9). The mobility is degraded with the counter-doping dose especially at low inversion charge and for nMOS, as expected by Coulomb scatterings. This is one of the main advantage of undoped channel FDSOI MOSFETs.

ANALOG PERFORMANCE

Concerning the analog applications, the main MOS performances are driven by the G_m/G_{ds} gain. The operating point for these circuits are often around a gate overdrive of V_g-V_{th}=0.2V and a drain current V_{ds}=V_{dd}/2. Fig. 11 shows the comparison of the analog gain G_m/G_{ds} for the short devices (for n and pMOS) between undoped and doped channel. Very good analog gains are obtained with undoped devices, which are at least 12% higher on nMOS and 25% on pMOS that the performance obtained with implanted channels.

Finally, the V_{th} mismatches of our devices are also addressed (Fig.12). As expected, the V_{th} fluctuations increase for FDSOI devices with doped channel, clearly demonstrating the dopant impurities impact on variability. More precisely, it is found that an implanted dose of 5 10^{12} at/cm^2 (As or BF_2) is enough to induce a 50% increase of the V_{th} fluctuations for both nMOS and pMOS. This is the main detrimental aspect of using counter-doping implants to tune the V_{th} in FDSOI MOSFETs.

CONCLUSION

In this paper, we demonstrate the tuning of the threshold voltage in thin FDSOI transistors with a high-k and single metal gate. A 10^{13} at/cm^2 counter-doping implantations in 10nm silicon thickness is efficient to induce a 200mV V_T lowering without significant degradation of the electrostatics. This demonstrates that Vth modulation by counterdoping could be a solution for multiple Vth integration on ultra-thin FDSOI technology.

ACKNOWLEDGEMENTS

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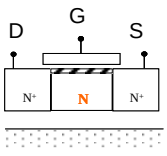
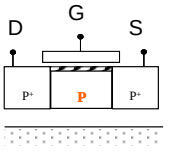


a: NMOS

NMOS
Arsenic
5E12at/cm^2=2E18at/cm^3
1E13at/cm^2=4E18at/cm^3
1,5E13at/cm^2=6E18at/cm^3
2E13at/cm^2=8E18at/cm^3



b: PMOS

PMOS
BF_2
5E12at/cm^2=2E18at/cm^3
1E13at/cm^2=4E18at/cm^3
1,5E13at/cm^2=6E18at/cm^3
2E13at/cm^2=8E18at/cm^3

Figure. 1: MOS structures in accumulation mode and summary of the different conditions used for the channel counter-doping Implantations

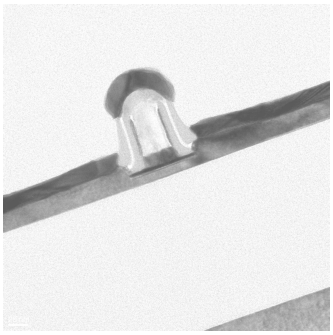


Figure. 2:. TEM cross section of a 30nm long FDSOI transistor.

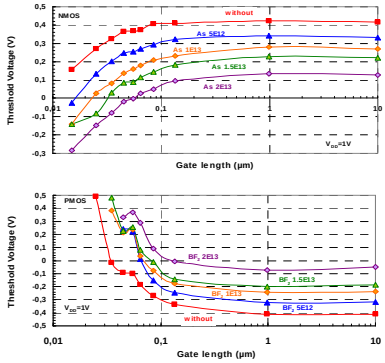


Figure. 3: Short channel effects for n & p MOS devices at VDD=1V

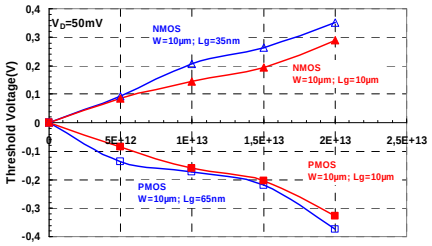


Fig. 4: Short and long MOS Vth shift as a function of the implanted dose (n&pMOS)

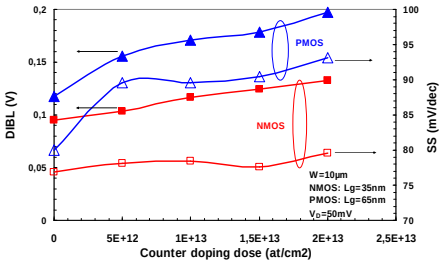


Fig. 5: DIBL and Subthreshold swing of Short MOS devices as a function of the implanted dose

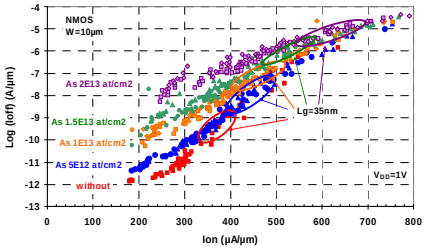


Fig. 6: Ion-Ioff trade-off for nMOS devices at VDD=1V.

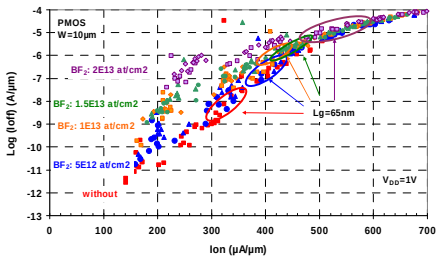


Fig. 7: Ion-Ioff trade-off for pMOS devices at VDD=1V

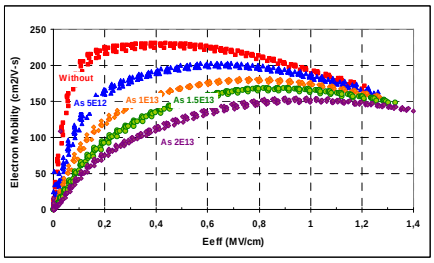


Fig. 8: Long channel electrons Mobility data as a function of effective field for various implanted dose.

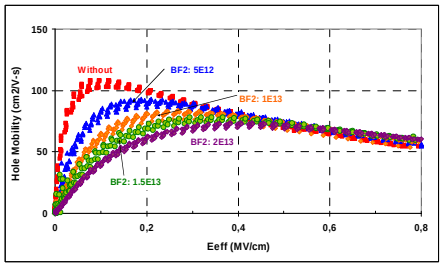


Fig. 9: Long channel holes Mobility data as a function of effective field for various implanted dose

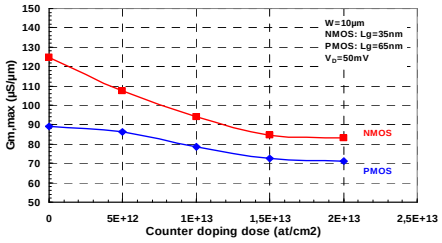


Fig. 10: Maximum of transconductance at VD=50mV as a function of the implanted dose

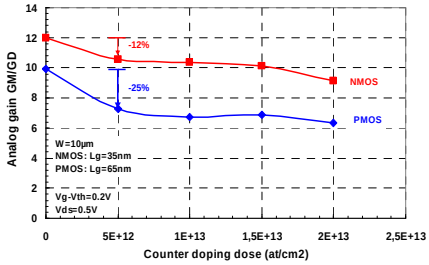


Fig. 11: Analog gain Gm/Gds for the short devices as a function of the implanted dose VDD=1V.

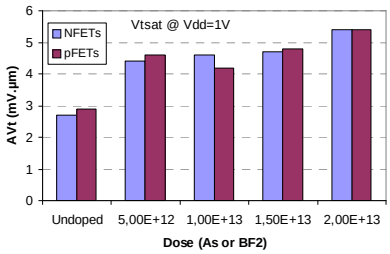


Fig. 12: Vth mismatch for nMOS and pMOS small areas at VDD=1V.