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High Performance (110)-oriented GOI pMOSFETs Fabricated by Ge Condensation Technique

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1. Introduction Recently, thin body Ge-On-Insulator (GOI) MOSFETs have attracted high attention as a promising candidate for CMOS devices towards 22 nm technology node and beyond. In addition, the combination of any mobility booster technologies with Ge channels is expected for further enhancement of the current drive. One of promising boosters is the choice of optimum surface orientation. It has been reported through theoretical calculations [1] that (110) surfaces can provide the maximum hole mobility in Ge p-MOSFETs. We have already reported the fabrication of ultrathin (110)-oriented GOI layers [2] by the Ge condensation method [3] and successful operation of the p-MOSFET [4]. While this was the first demonstration of planer (110)-oriented GOI p-MOSFETs, the device characteristics and the mobility behaviors have not been presented yet. In this work, we present the electrical characteristics of (110) and (100)-oriented GOI pMOSFETs with emphasis on the surface orientation and the temperature dependence of the mobility and the sub- threshold slope.

2. Samples and Measurement Method Fig. 1 illustrates the fabrication processes of (110) and (100)- oriented GOI pMOSFETs. The fabrication process started from MBE growth of SiGe (x=30 %, 40 nm) and Si layers on (110)-oriented SOI wafers, following a formation of thin SiO_2 cap at low temperature oxidation (a). Next (b), the Ge condensation was carried out until the Ge content (Fig. 2) was confirmed to be 100% by Raman spectrometry. After the device isolation and stripping off the top SiO_2 layers, atomic hydrogen annealing was carried out at 450°C in order to terminate channel defects generated during the Ge condensation process[5]. Next, the formation of Pt-Germanide source/drain was carried out by deposition of a thin Pt film followed by forming gas annealing at 400°c for 30 minutes. Finally, thin Al films were deposited for forming gate electrodes of the back gate structure (c). As for (100)-oriented GOI p-MOSFETs the only difference is to use (100)-oriented SOI wafers as starting substrates.

3. Results Fig. 2 shows the Raman measurements of the resultant (110) and (100)-oriented GOI layers. The only availability of Ge-Ge mode peaks confirms the formation of GOI layers. The surface orientations were confirmed by X-ray diffraction. The estimated channel thickness of the both GOI layers from TEM images in Fig. 3 was 12 nm.

Fig. 4 shows the change in I_d-V_g characteristics of (110) GOI p-MOSFETs by atomic hydrogen annealing. The dramatic reduction in the off current is attributable to hydrogen termination of channel defects generated during the Ge condensation. Fig. 5 and 6 demonstrate the successful device operations on the both surface orientations. Here, the gate voltage was adjusted for comparison so as to provide same surface carrier concentrations, since the thickness of BOX is 145 and 50 nm for (110)- and (100)-oriented GOI p-MOSFETs, respectively. It is found that (110) GOI p-MOSFETs have higher drain current than (100) ones.

The I_d-V_g characteristics of (110)- and (100)-oriented GOI p-MOSFETs are shown as a parameter of the measurement temperature in Fig. 7 and 8, respective. It is found that I_{on}/I_{off} ratio more than 10^5 can be obtained even at 300 K for the both orientations. However, the sub-threshold slope of (110) GOI p-MOSFETs is much higher than that of (100) ones. Fig. 9 shows the temperature dependence of the sub-threshold slopes of the both orientations. A linear relationship between the sub-threshold slopes and temperature means that the sub-threshold slopes of the GOI MOSFETs obey to the conventional theory of carrier conduction in the sub-threshold region and, thus, that the different sub-threshold slopes between (110) and (100) are attributed to higher interface trap density (D_{it}) at the (110) Ge/BOX interface. The estimated D_{it} values are 1.4×10^{13} and 8×10^{12} ($eV^{-1}cm^{-2}$) for the (110) and (100) MOSFETs, respectively.

Hole mobility was evaluated through integrating C-V curves of MOSFETs from the threshold voltage. Fig. 10 shows the channel direction dependence of the hole mobility on (110)-oriented GOI p-MOSFETs. Here, the angle means the one tilted from <100> direction. Thus, channel direction with 90 degrees corresponds to <110>. It is found experimentally, for the first time, that <110> channel provides the highest hole mobility on (110)- oriented GOI layers [4, 5], being almost twice higher than <100> direction.

Fig. 11 and 12 show the hole mobility of (110) and (100) GOI p-MOSFETs, as a parameter of temperature. It is found at 300K that (110) GOI p-MOSFETs have 3 times higher hole mobility than the Si universal hole mobility, while (100) GOI p-MOSFETs have 1.3 time higher hole mobility, meaning the superior performance of (110) GOI p-MOSFETs. In low effective field region, (110) GOI p-MOSFETs have lower hole mobility than the Si hole mobility with weak temperature dependence. Also, the mobility increases with an increase in E_{eff}. These facts strongly suggest the influence of Coulomb scattering. In contrast, these characteristics of Coulomb scattering are not clearly seen in the mobility on (100). This stronger influence of Coulomb scattering on the (110) GOI mobility is attributed to the higher interface trap density at (110) GOI/BOX interfaces. Fig. 13 shows the ratio of the (110) GOI mobility to the (100) one as a function of temperature. The ratio increases with an increase in N_s. The mobility ratio at N_s of $1x10^{13}$ cm^{-2} is found to amount to 2.4. This value is much higher than the theoretical prediction, 1.6 [1].

4. Summary The electrical characteristics of (110)-oriented GOI p-MOSFETs have been demonstrated. (110)-oriented GOI p-MOSFETs along <110> direction have exhibited 3 time and 2.4 time higher hole mobility than the Si and the (100) GOI hole mobility, respectively, providing strong evidences that (110)/<110> Ge channels are promising for future high performance MOSFETs.

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References: [1] T. Krishnamohan et al., IEDM Tech. Dig., pp. 899-902(2008) [2] S. Dissanayake et al., ICSI-5, pp. 57-58 (2007) [3] S. Dissanayake et al., Thin Solid Films, Vol. 517(1), pp. 178-180 (2008) [4] S. Nakaharai et al.,Appl. Phys. Lett., Vol. 83, pp. 3516-3518, (2003).[5] S. Dissanayake et al., ISSCC-5,pp. 233-234 (2007) [6] T. Low et al., Elect. Dev.,Vol. 52(11), pp. 2430-2439 (2005)

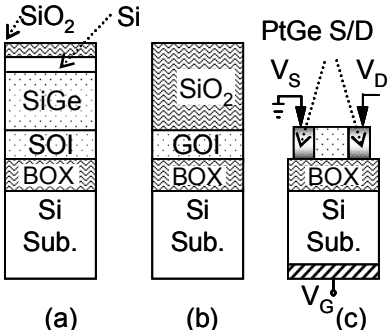

Fig. 1 Fabrication process of GOI pMOSFETs

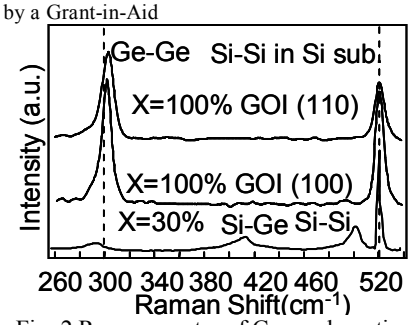

Fig. 2 Raman spectra of Ge condensation

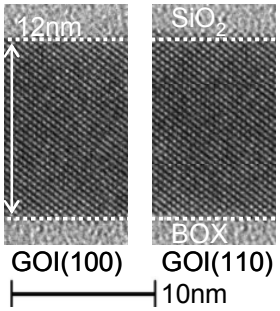

Fig. 3 TEM images of GOI layers

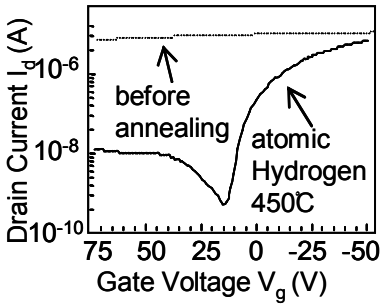

Fig. 4 The effect of atomic H annealing

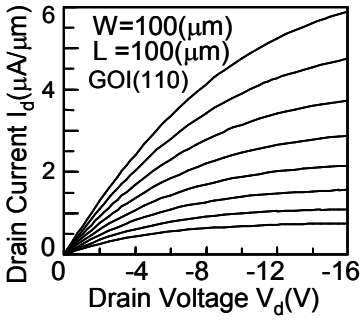

Fig.5 I_d-V_d characteristics of (110)GOIpMOSFETs.$(V_g-V_{th})/t_{BOX}$;-1.66 to-0.69(MV/cm) step:0.14(MV/cm)

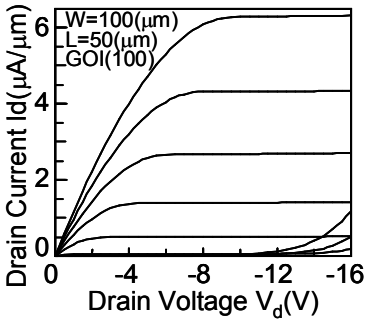

Fig.6 I_d-V_d characteristics of (100)GOIpMOSFETs.$(V_g-V_{th})/t_{BOX}$;-1.66 to-0.69(MV/cm) step:0.14(MV/cm)

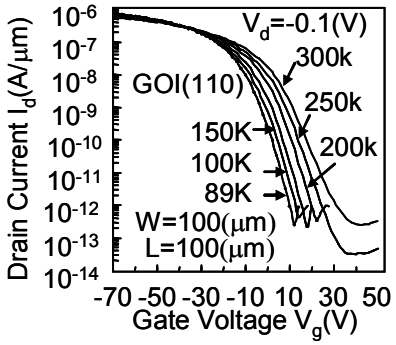

Fig.7 Temperature dependency on I_d-V_g characteristics of (110)GOI pMOSFETs

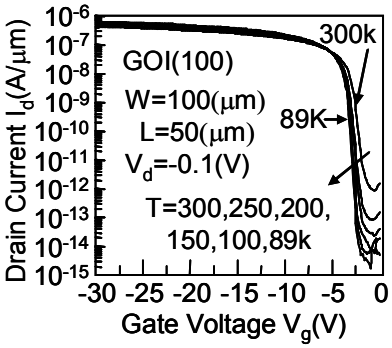

Fig.8 Temperature dependency on I_d-V_g characteristics of (100)GOI pMOSFETs

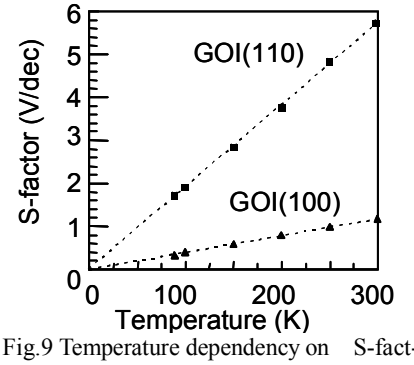

Fig.9 Temperature dependency on S-factors of (110)and (100) GOI pMOSFETs

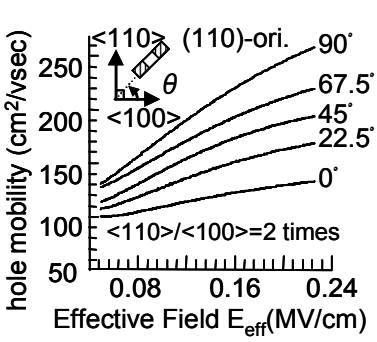

Fig.10 Channel direction dependency on hole mobility on (110)-oriented GOI pMOSFETs

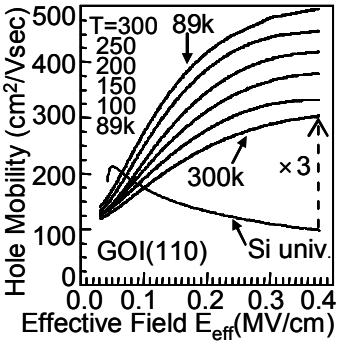

Fig.11Temperature dependency on hole mobility of (110) GOI pMOSFETs

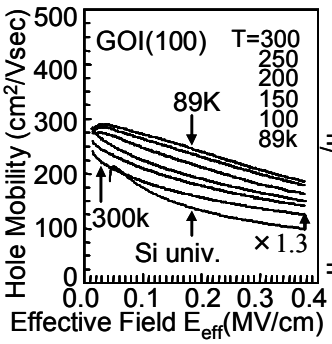

Fig.12 Temperature dependency on hole mobility of (100) GOI pMOSFETs

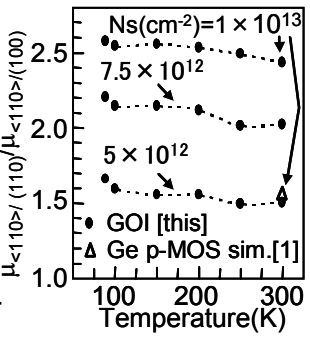

Fig.13 mobility enhancement depencency on temperature and surface hole concentration