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Channel-Proximate Silicon-Carbon Source/Drain Stressors for Performance Boost in Strained N-Channel Field-Effect Transistors

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ABSTRACT

We report the demonstration of a novel integration scheme for realizing strained n-FETs with enhanced strain effects by deploying silicon-carbon (Si:C) source/drain (S/D) stressors in close proximity to the channel, i.e. Channel-proximate (CP) Si:C S/D stressors. The Si:C S/D is formed by carbon implant and solid phase epitaxy (SPE). Details of the process technology and integration scheme will be discussed. A high substitutional carbon concentration C_{sub} of 1.5% is achieved. N-FETs with Si:C S/D show 8% drive current enhancement over control devices. At a given I_{OFF}, I_{On} of n-FETs with CP Si:C S/D is improved by 6% over n-FETs with non-proximate Si:C S/D and 14% over Si S/D control.

INTRODUCTION

Strained engineering has been a workhorse in IC manufacturing to increase carrier mobility and transistor drive current. Beyond the 32 nm technology generation, further increase in the strain level in the Si channel will be required to enhance device performance. Recently, embedded Silicon-Carbon (e-Si:C) source/drain (S/D) stressors has gained significant attention for n-FET performance enhancement [1]-[7]. Si:C S/D can be formed by C^+ implant followed by solid phase epitaxy (SPE) in the S/D region of n-FETs [4],[5]. To further increase the strain effect of Si:C S/D stressors, higher substitutional carbon concentration C_{sub} has to be achieved in the S/D regions. However, presence of high C concentration will result in carbon-induced dopant deactivation leading to a high sheet resistance R_s which is a potential issue, especially in aggressively scaled transistors where parasitic resistance is important.

In this paper, an advanced Si:C S/D formation technology was developed to form strained n-FETs with channel-proximate Si:C S/D stressors, placed in close proximity to the channel for enhanced strain effects. A high substitutional carbon concentration (C_{sub}) of 1.5% was achieved. Significant performance enhancement was observed.

CHANNEL-PROXIMATE Si:C S/D (CP Si:C): INTEGRATION

Key process steps for the two device splits are shown in Fig. 1: n-FET with Si:C formed after spacer, and n-FET with Si:C in close proximity to the channel for enhanced strain effects [called channel-proximate (CP) Si:C S/D]. After definition of active regions, well implant, threshold voltage V_t adjust implant, and anti-punchthrough implant were performed. For CP Si:C S/D n-FETs, C implantation was performed through a 10 nm sacrificial oxide after poly-Si/SiO_2 gate stack formation. Si:C stressors and S/D extension (SDE) were then formed before spacer formation. For non-proximate Si:C n-FET, implantation of C into the S/D region was performed after spacer formation. For all Si:C devices, C implantation was carried out using cold implant for reduced implant damage. P^+ was used in the deep S/D region for improved R_s or S/D activation and a 2-step SPE anneal was carried out to form the Si:C S/D stressors [6]. A 30 nm thick SiO_2 layer was deposited prior to SPE anneal to minimize possible carbon out-diffusion. An unstrained control n-FET with Si S/D was also fabricated. A 2-step silicidation process was carried out for all devices. Fig. 2 shows a transmission electron microscopy (TEM) image of an N-FET with CP Si:C S/D. The spacer critical dimension was targeted to be ~25 nm for all devices. Full restoration of the crystalline quality is observed in the TEM image. Formation of high-quality Si:C in the S/D region is required for its application as stressors.

RESULTS AND DISCUSSION

A. Superior C_{sub} and Strain Level in CP Si:C S/D n-FETs

Impact of dopants on C_{sub} was first investigated. Different amount of P^+ was introduced into C containing samples before SPE anneal (800°C 40s followed by 650°C 2min) was carried out. High-resolution X-ray diffraction (HRXRD) was used to quantify C_{sub}, and revealed that lower C_{sub} was achieved in samples where higher concentration of P^+ was introduced (Fig. 3). This is due to the enhanced substitutional-to-interstitial diffusivity of C in presence of P^+ during thermal processing [5]. Next, to investigate C_{sub} formed in CP Si:C S/D n-FETs, different SPE conditions were tested: Furnace anneal at 720°C 2 hr, RTA at 800°C 40 s and RTA followed by furnace anneal. The furnace anneal condition was chosen to match the thermal budget of spacer formation. It was observed that SPE by RTA resulted in slightly higher C_{sub} as compared to SPE by furnace anneal (Fig. 4). Note that there is minimal loss in C_{sub} in samples which underwent both RTA and furnace anneal. As this annealing condition is similar to the thermal budget experienced during the formation of CP Si:C S/D n-FETs, this suggests that C_{sub} achieved in the formation of CP Si:C S/D n-FETs remained relatively stable even after spacer formation. Fig. 5 shows that high C_{sub} can be achieved in regions where the concentration of dopants is low (i.e. regions beneath SDE region) as compared to regions where the concentration of dopants is high (i.e. deep S/D regions). This indicates that CP Si:C S/D may have higher C_{sub} as compared to non-CP Si:C S/D. Higher C_{sub} and close proximity of the Si:C stressors to the channel is vital for boosting the strain effect.

B. Performance Booster with CP Si:C S/D

We integrated the new Si:C formation process in a n-FET process flow and performed a statistical comparison of device performance. Fig. 6 compares the I_{On}-I_{Off} of n-FETs with CP Si:C S/D, Si:C S/D and Si S/D. At an I_{OFF} of 300 nA/μm, I_{On} enhancement is 6% and 14% for CP Si:C S/D n-FETs over Si:C S/D and Si S/D n-FETs, respectively. I_{On} versus Drain-induced barrier lowering (DIBL) plot (Fig. 7) shows a ~12% enhancement for CP Si:C S/D over control devices at a DIBL of 150 mV/V. As DIBL is related to the short channel effect and effective channel length, comparing I_{On} enhancement at the same value of DIBL illustrates the enhancement at almost the same effective channel length. Fig. 8 shows the cumulative probability plots of the junction leakages for all devices. Comparable junction leakages are observed for all devices. A matched pair of CP Si:C S/D and Si S/D n-FETs were examined more closely. Fig. 9 shows the transfer characteristics of the matched pair where both the devices have a DIBL of 140 mV/V and SS of 113 mV/dec, indicating they have the same effective channel length. S/D series resistance for n-FETs with CP Si:C S/D and Si S/D are examined from the asymptote in the R_{TOTAL}-V_G curve (Fig. 9 inset). The series resistance of the CP Si:C S/D n-FETs is ~10% higher than that of the Si S/D control probably due to slightly lower activation of As^+ in the SDE. Despite a higher series resistance, I_{DS}-V_{DS} plots for n-FETs with CP Si:C S/D shows enhancement in I_{DS} over Si:C S/D n-FETs (Fig. 10). I_{On} of strained CP Si:C S/D n-FETs can be further enhanced by integrating it in [010]-oriented devices (Fig. 11). This is attributed to the anisotropic electron population at the Δ_4 valleys which results in smaller conductive mass and thus higher mobility enhancement.

CONCLUSION

Successful integration of Si:C S/D stressors in close proximity to the channel was found to boost the strain effect. Channel-Proximate Si:C S/D stressors gave 14% I_{On} enhancement for control devices. Comparable junction leakage, SS and DIBL were obtained. Further I_{On} enhancement can be achieved by using CP Si:C S/D for [010]-oriented devices.

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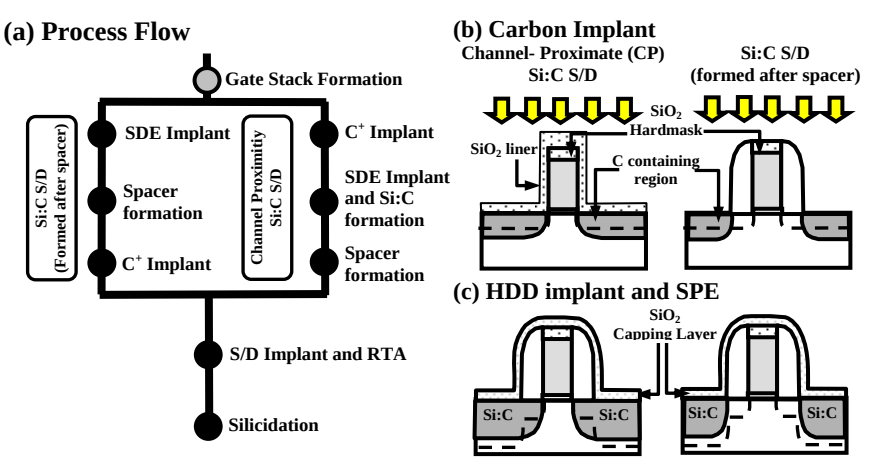

Fig. 1. (a) Key process steps employed in this work, including (b) carbon (C^+) to form Si:C S/D in close proximity to the channel, and SPE to form (c) n-FET with Si:C S/D stressors.

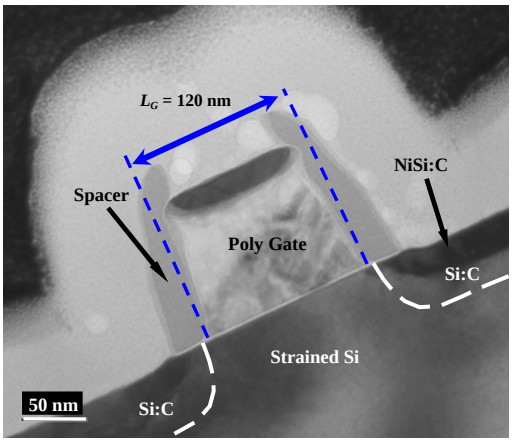

Fig. 2. TEM image of the sample implanted with carbon. After SPE, full restoration of the crystalline quality is achieved as seen in the TEM image. C_{sub} of 1.5% is achieved for CP Si:C S/D n-FET.

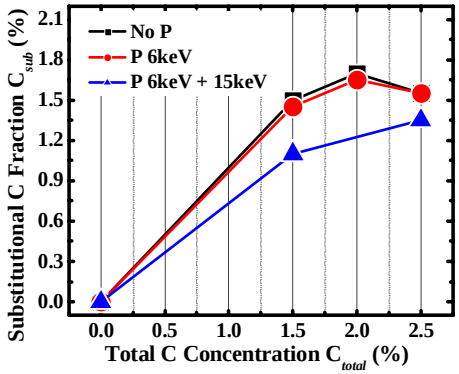

Fig. 3. Increasing amount of P^+ enhanced substitutional-to-interstitial diffusivity of C.

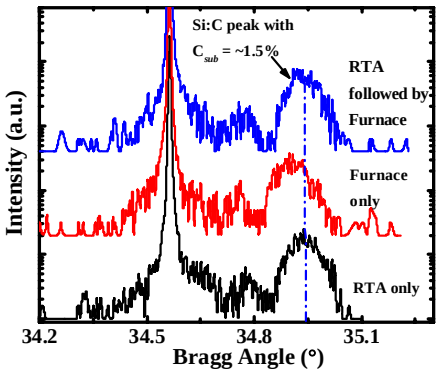

Fig. 4. Minimal loss in substitutional carbon after spacer formation.

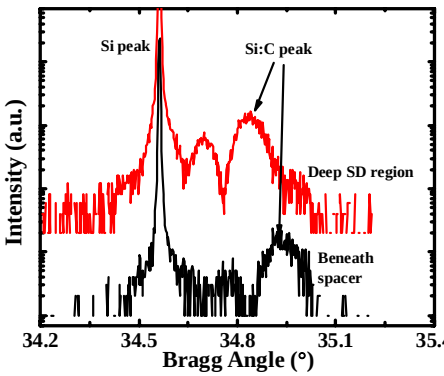

Fig. 5. Higher C_{sub} can be achieved in CP Si:C S/D n-FETs due to lesser dopant interaction.

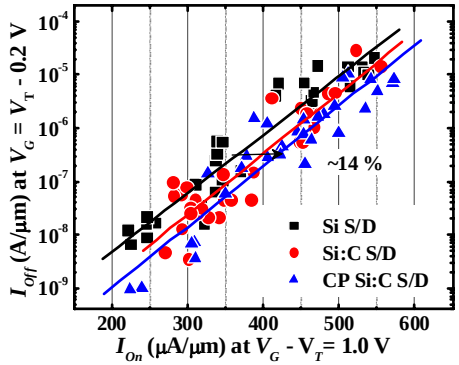

Fig. 6. At I_{OFF} = 300 nA/μm, n-FET with CP Si:C S/D has 14% higher I_{On} than Si S/D n-FET.

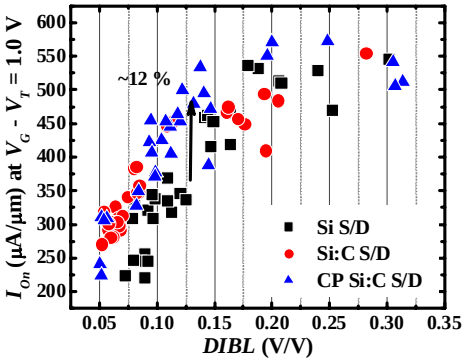

Fig. 7. At DIBL of 0.15 V/V, n-FET with CP Si:C S/D shows enhancement in I_{On} of 12% over control.

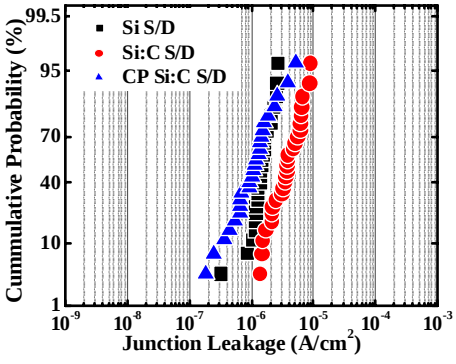

Fig. 8. Cumulative probability plot showing comparable junction leakages for all devices.

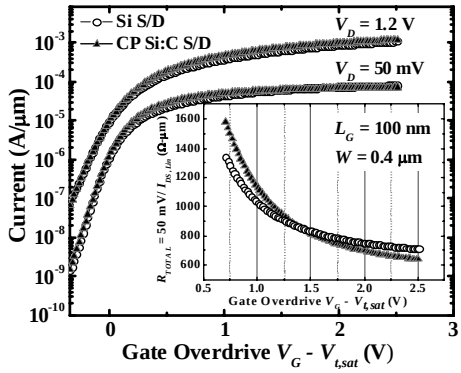

Fig. 9. I_{DS}-V_{GS} curves for CP Si:C n-FETs or Si S/D show comparable DIBL and subthreshold swing. (inset) Si S/D n-FETs shows lower series resistance than CP Si:C S/D n-FETs.

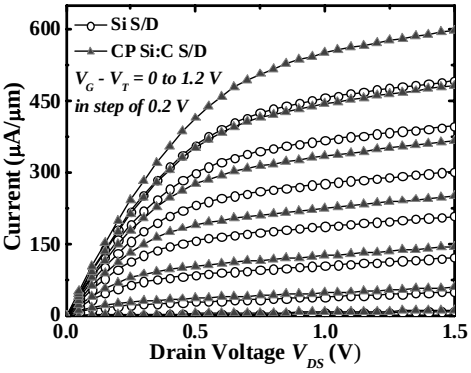

Fig. 10. Device with channel-proximate Si:C S/D shows enhancement in I_{DS} over devices with Si:C S/D.

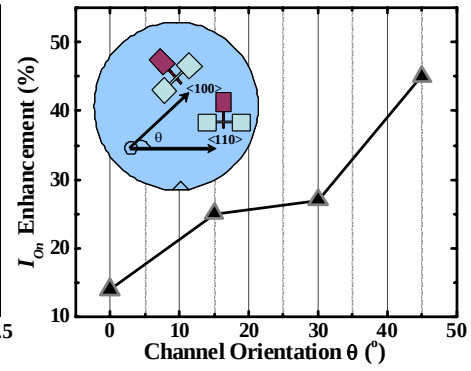

Fig. 11. Highest I_{On} enhancement observed for [010]-oriented CP Si:C n-FETs, consistent with the directional dependence of piezoresistance coefficients.