Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp20-21

The Tunnel Source n-MOSFET: A Novel Asymmetric Device for Low Power Applications

Venkatagirish N.[1], Ahmet Tura[1], Ritesh Jhaveri[1], Hsu-Yu Chang[1] and Jason Woo[1]
[1]Department of Electrical Engineering, University of California, Los Angeles, CA 90095, USA
Phone: +1-(310) 206 3279 E-mail: woo@ee.ucla.edu

1. Introduction

As MOSFETs are aggressively scaled, their performance is severely limited by short channel effects (DIBL and V_{TH} roll-off), off-state and gate leakages, parasitic capacitances and resistances, etc. These, in addition to V_{DD} scaling limitation and high sub-threshold swing (>60mv/dec) give rise to high I_{OFF} and make power dissipation an enormous challenge, especially for low power/low current applications. New device innovations are essential to achieve low I_{OFF} and high g_m with high R_{OUT} for digital and analog applications, respectively. Tunnel FETs (TFETs) [1-2] can potentially achieve sub-60mV/dec subthreshold swing (SS) and operate at lower V_{DD}, since source injection is dictated by band-to-band tunneling instead of diffusion. Most TFETs suffer from I_{ON} degradation and high average SS close to V_{TH}. To overcome these problems, we have proposed the Tunnel Source (PNPN) n-MOSFET [3], as shown in Fig. 1. This novel asymmetric device has the potential for steep sub-threshold behavior, improved I_{ON}/I_{OFF}, high R_{OUT} and gain (g_m x R_{OUT}) at low bias currents. It also possesses excellent immunity against short channel effects which improves scalability into sub-50nm regime and makes it an attractive candidate for low power digital and analog operations.

2. Concept of Tunnel Source (PNPN) n-FET

The proposed nFET as shown in Fig. 1 has a p^+ source and the current is controlled by band-to-band tunneling between the source and the channel, which is governed by the Fermi selection rule, the tunneling barrier height (ϕ_{TUN}) and width (W_{TUN}) [3]. The band diagram for the tunnel FET in the OFF-state and the ON-state are shown in Fig. 2 (a) and (b) respectively. To reduce the tunnel junction resistance, a smaller bandgap source material (SiGe) has been proposed previously to lower ϕ_{TUN} [4]. However, it is also necessary to reduce W_{TUN}. In our proposed structure, the thin fully depleted n^+ layer increases the lateral electric field and therefore reduces $W_{TUN,}$ minimizing the potential drop across the tunneling junction and therefore improving I_{ON}. The sub-threshold swing is minimized when the pocket is *just* fully depleted as shown in band diagram or when the tunneling distance is just equal to the pocket width.

3. Device Performance

Fig. 3 shows the comparison between the I-V characteristics for a Tunnel Source (PNPN) n-MOSFET and corresponding conventional SOI MOSFET with the same structural parameters (L_G=90nm, T_{OX}=25Å, T_{SI}=60nm at the same I_{OFF} = 10pA/µm. Pocket width=4nm, Pocket doping=$5x10^{19}cm^{-3}$). The simulations have been performed with ATLAS device simulator, calibrated with experimental data obtained from silicon tunnel diodes [3]. With a narrow (~4nm) n^+ region, the PNPN n-MOSFET shows a steep sub-threshold behavior (SS~30mv/dec over 3-4 decades at 300K) with low I_{OFF}. This is highly beneficial for low standby power applications.

Fig. 4 shows the behavior of subthreshold swing vs. V_{GT}. It is seen that for the tunnel FET with pocket width 4nm the swing goes below the diffusion limit of 60mV/dec for a wide range. The n^+-pocket has to be just fully depleted, which is crucial for beneficial device operation. For a wider pocket with the same doping, the pocket is partially depleted; therefore the device is diffusion limited and behaves like a conventional SOI MOSFET (Fig. 4). The band diagrams shown in Fig. 5 (a) - fully depleted pocket and Fig. 5 (b) - partially depleted pocket, show this clearly. Thus, fully depleted n^+ layer is essential for the device to achieve steep sub-threshold behavior and high I_{ON}.

Excellent robustness to SCEs provided by the PNPN n-MOSFET can be seen in Fig. 6 where the DIBL and V_T roll-off are reduced as the channel length decreases. This is due to negligible source-to-channel coupling and reduced influence of drain bias on the source tunneling junction. This is particularly favorable for low standby power where the I_{ON}/I_{OFF} ratio as well as low I_{OFF} is maintained with scaling to sub-50nm gate lengths

The tunneling injection mechanism, negligible DIBL and improved resistance to SCEs of the PNPN n-MOSFET have favorable implications for low operating power (low I_{BIAS}) analog applications as well. Fig. 7 shows that the transconductance (g_m) of the Tunnel Source n-MOSFET for a just-fully depleted pocket width of 4nm is higher as compared to the conventional SOI device, at low I_{BIAS} (V_D = 0.8V), due to the tunneling injection mechanism at the source. (g_{mSAT} is still lower than the conventional SOI) .

Fig. 8 shows that the PNPN n-MOSFET exhibits an improvement in R_{OUT} over the conventional SOI for the given channel length. This can be attributed again to reduced drain coupling (DIBL) and resistance to SCEs. When channel length decreases the R_{OUT} is governed by DIBL, rather than channel length modulation. As a result, the intrinsic gain (g_m x R_{OUT}) of the PNPN n-MOSFET is also higher than the conventional device, especially at low bias currents, as shown in Fig. 9

4. Conclusions

The novel Tunnel Source (PNPN) n-MOSFET is highly promising for stand-by power reduction as it can decrease the subthreshold swing and I_{OFF} beyond the limits for conventional devices. It also shows excellent short channel immunity, significantly higher g_m, R_{OUT} and intrinsic gain in addition to good high frequency characteristics, especially at low I_{BIAS}.

Acknowledgements

The authors would like to acknowledge and thank DARPA for providing funding for the project.

References

[1] T. Krishnamohan, et al, p. 947 (2008).
[2] F. Mayer et al, *IEDM*, p. 163 (2008)
[3] Venkatagirish N. et al, *TED* Vol. 55, No. 4, p. 1013 (2008)
[4] K. K. Bhuwalka, et al, *TED*, Vol. 52, No. 7, p. 1541 (2005)

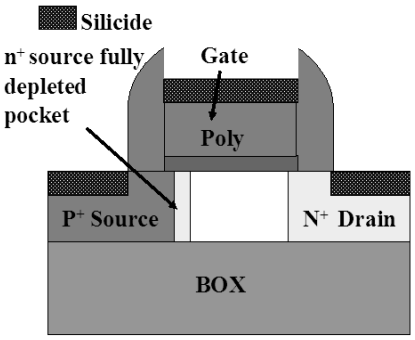

Fig. 1 Device structure of the tunnel source (PNPN) n-FET

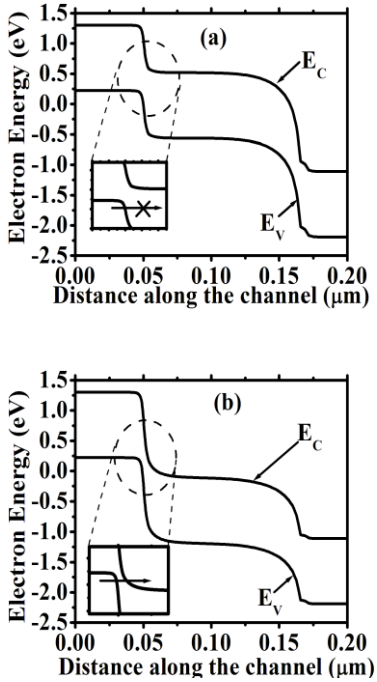

Fig. 2 Band Diagram of the tunnel n-FET in the (a) OFF state and (b) ON state

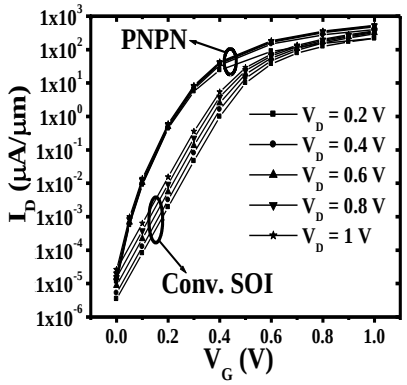

Fig. 3 Comparison of I_D-V_G curves for the PNPN tunnel FET and Conventional SOI MOSFET. The tunnel FET shows <60mV/dec subthreshold swing

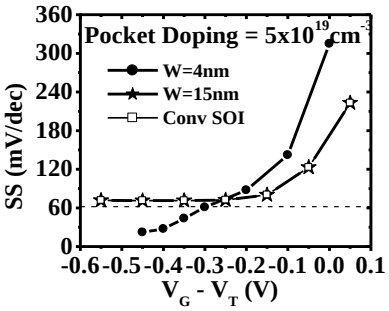

Fig. 4 SS vs V_{GT} for the tunnel n-FET with 2 widths and conv. SOI n-FET. When W = 4nm (fully depleted) the SS goes below 60mV/dec

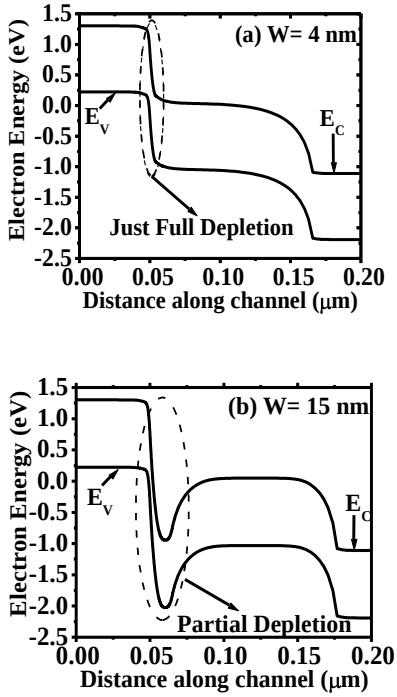

Fig. 5 Band diagram when the pocket is (a) fully depleted and (b) partially depleted

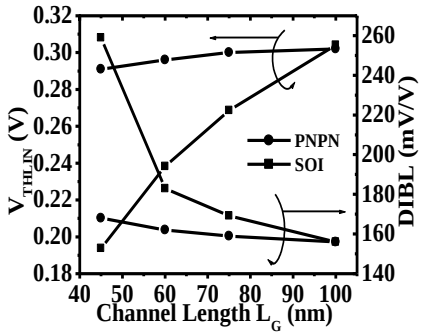

Fig. 6 Scaling of the tunnel n-FET with respect to V_{Th} roll off and DIBL

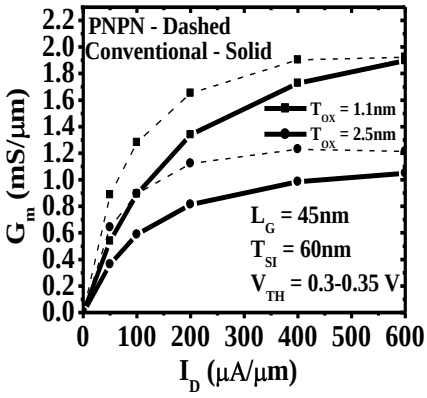

Fig. 7 Transconductance of the PNPN tunnel FET in comparison to conv. SOI n-FET. The tunnel n-FET has higher transconductance due to tunneling injection mechanism

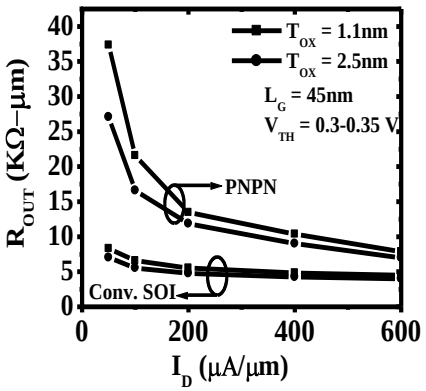

Fig. 8 Comparison of output resistance of the PNPN tunnel FET and conv. SOI n-FET

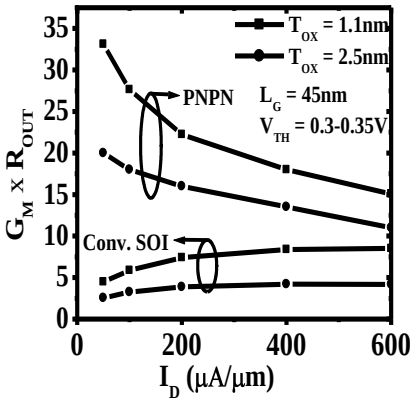

Fig. 9 Comparison of the intrinsic gain of the PNPN tunnel FET and the conv. SOI n-FET. The tunnel n-FET has higher gain performance.