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Temperature Coefficient of Threshold Voltage in Metal/High-k Gate Transistors with Various Thickness of TiN and Capping Layers

Y. Nishida[1, 2], K. Eikyu[1], A. Shimizu[1], T. Yamashita[1], H. Oda[1], Y. Inoue[1], and K. Shibahara[2,3]
[1] Renesas Technology Corp., 4-1 Mizuhara, Itami, Hyogo, 664-0005, Japan
[2]Graduate School of Advanced Science of Matter, Hiroshima University
[3]Research Institute for Nanodevice and Bio Systems, Hiroshima University
Phone: +81-72-787-2376, Fax: +81-72-789-3438, E-mail: nishida.yukio@renesas.com

Abstract
Temperature coefficient of V_{th} (=dV_{th}/dT) in metal gate nFET with various thickness of TiN and capping layer was systematically obtained. Thick TiN metal or thick Al_2O_3 capping in gate stack structures enhanced dV_{th}/dT due to increase in EOT. Thick TiN devices showed lager shift in V_{FB}, which was one of the origins of enhanced dV_{th}/dT. In contrast, La_2O_3 capping scarcely affected dV_{th}/dT.

1. Introduction

For suppression of gate leakage current and to increase drive current, advanced high-k/metal gate transistors, especially gate-first metal gate transistors which are compatible with a conventional fabrication process flow, are under development [1-2]. The gate first devices are attractive for low stand-by power application because of their cost effectiveness. A schematic crosssection of a typical metal gate transistor is shown in Fig.1. V_{th} is adjusted by a capping layer on the high-k insulator. La-capping and Al-capping to lower the V_{th} [3-5] are most popular for nFET and pFET, respectively. TiN deposited on the capping layer is also available for V_{th} adjustment, since the eWF (effective work-function) can be modulated by TiN tchickness [6].

It is desirable for integrated circuit that V_{th} shift between room temperature and operating temperature is negligible. However, V_{th} varies depending on operating temperature and its temperature coefficient(dV_{th}/dT) is commonly utilized for circuit design, Recently it was reported that dV_{th}/dT of metal gate transistors were larger than that for conventional poly-Si gate transistors [7-8]. Different from high performance devices used with temperature management, low stand-by power devices are often demanded stable operation under wide temperature range, assuming usage in very cold outdoor in winter and very hot heated automobiles under summer sunshine. If the value of $|dV_{th}/dT|$ is large, even if I_d is increased by metal gate, circuit designers cannot make the most of device performance to keep large function-margin for the hot and the cold environments. Although the temperature coefficient of V_{th} is thus important for the gate first metal gate devices, discussion combined with eWF was not sufficient yet. Therefore, influences of TiN thickness and and capping conditions are described in this paper.

2. Experiment

Basic conditions of devices fabricated for this work are summarized in table I. All samples were fabricated with the same substrate concentration and the same high-k gate insulator. All devices were nFETs to unify substrate doping condition and to make discussion simple. V_{th} was modified by the La_2O_3 capping or the Al_2O_3 capping on the high-k insulator. In addition, V_{th} was also adjusted by TiN thickness. TiN was deposited by two methods, CVD or PVD. After the TiN deposition, all samples passed through the same fabrication processes.

Figures 2-4 indicate the V_{th} shift and EOT shift of the fabricated nFET samples. Figure 2 shows the dependence of TiN thickness. Although TiN for samples A and B were deposited by different methods, they have the same tendency. Thick TiN increased eWF and raised V_{th} [6]. Thick TiN also increased the EOT, which is possibly attributable to oxygen contained in TiN. Dependence of La_2O_3 thickness is indicated in Fig.3. Although V_{th},was largely lowered by thick La_2O_3, EOT was hardly changed. Figure 4 shows V_{th} change for Al_2O_3 capped FETs. V_{th} shifted higher due to larger eWF and EOT for thicker Al_2O_3.

3. Result and Discussion

V_{th} of nFET (L_g=1μm) was measured in linear region at several temperatures, and the temperature coefficient (=dV_{th}/dT) at 25°C was calculated.

The results are indicated in Fig.5. Because dV_{th}/dT has negative value, the low value of dV_{th}/dT means the large value of $|dV_{th}/dT|$, which indicates large change width caused by certain change of temperature. Figure 5(a) shows TiN thickness dependence of dV_{th}/dT. Regardless of the difference of deposit methods, thick TiN metal gate has large absolute value of temperature coefficient of V_{th}. La_2O_3 and Al_2O_3 capping thickness dependences of dV_{th}/dT is shown in Fig.5 (b). The temperature coefficient increases with Al_2O_3 thickness and scarcely depends on the La_2O_3 thickness.

V_{th} is expressed as $$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a\phi_f}}{C_{ox}} \quad \text{----(1)}$$

Here, V_{FB} is flat band voltage, ϕ_f is difference of potential from the intrinsic Fermi level, q is elementary charge, $\varepsilon_0\varepsilon_{Si}$ means dielectric constant of Si, N_a is substrate concentration, and C_{ox} is gate capacitance. Because all samples have the same substrate condition, it is thought that there is no difference in behavior of the second term of equation (1) among the samples. Therefore, if the effects from the first term and the third term in equation (1) are considered, analysis of characteristics of dV_{th}/dT is sufficient.

The temperature coefficient of the first term, which means temperature coefficient of V_{FB}, was calculated from C-V measurement, and the results are indicated in Fig.6. TiN thickness dependences of dV_{FB}/dT are shown in Fig.6 (a). The sample with thick TiN changes temperature coefficient to negative direction like Fig.5 (a). Therefore, some of the change of dV_{th}/dT to negative direction shown in Fig.5 (a) is explained by the effect of dV_{FB}/dT, the first term of equation (1). Capping thickness dependences of dV_{FB}/dT are shown in Fig.5 (b). The difference between the level of samples C (La_2O_3) and the level of samples D (Al_2O_3) comes from the difference of TiN thickness (4nm in samples C, 15nm in samples D). In contrast, the shifts caused by Al_2O_3 thickness or La_2O_3 thickness are relatively small compared to the shifts by TiN thickness indicated in Fig.6 (a). From these results, it is thought that the effect of the first term of equation (1), the temperature coefficient of V_{FB}, is increased with TiN thickness.

Because the effect of the third term of equation (1) is the other factor which affects the value of dV_{th}/dT, the effect of the third term is estimated by $dV_{th}/dT–dV_{FB}/dT$ (the difference between Fig.5 and Fig.6). It is plotted in Fig.7. TiN thickness dependences of $d(V_{th}–V_{FB})/dT$, which is shown in Fig.7 (a), are more gradual compared to dV_{th}/dT shown in Fig.5 (a). In addition, the difference of $d(V_{th}–V_{FB})/dT$ between La_2O_3 and Al_2O_3, which is shown in Fig.7 (b), is smaller than the difference of dV_{th}/dT in Fig.5 (b). These are explained that when the TiN thickness is changed, some of the change of dV_{th}/dT is attributed to the change of dV_{FB}/dT. Figure 8 is the correlation between EOT and $d(V_{th}–V_{FB})/dT$, which means the effect of the third term of equation (1), of all samples in this work. Because the value of $sqrt(4q\varepsilon_0\varepsilon_{Si}N_a\phi_f)$, which means depletion charge, is common among all samples, the value of the third term is affected only by $1/C_{ox}$. Therefore, $d(V_{th}–V_{FB})/dT$ is determined by EOT thickness as shown in Fig.8. Because reduction of EOT thickness suppresses the effect of the third term of equation (1), it is effectual to reduce the value of $|dV_{th}/dT|$.

4. Conclusions

The temperature coefficient of V_{th} (=dV_{th}/dT) is affected by TiN thickness and EOT thickness. Thick TiN is thought to enhance the temperature coefficient of V_{FB}. Thick EOT enhances the influence to V_{th} from the depletion charge. To suppress the temperature coefficient of V_{th}, gate stack structure with thin TiN layer and thin EOT is desirable. In addition, it is necessary to control V_{th} without increase of EOT.

References

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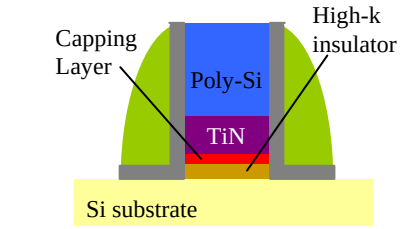


Fig.1 The schematic diagram of the samples of this work. The eWF depends on TiN thickness and the condition of the capping layer, La_2O_3 or Al_2O_3.

	TiN		Capping
	Process	Thickness	
Samples A	CVD	4 or 15nm	Non
Samples B	PVD	4 or 15nm	Non
Samples C	PVD	4nm	La_2O_3
Samples D	PVD	15nm	Al_2O_3

Table I Conditions of the nFET samples fabricated in this work.

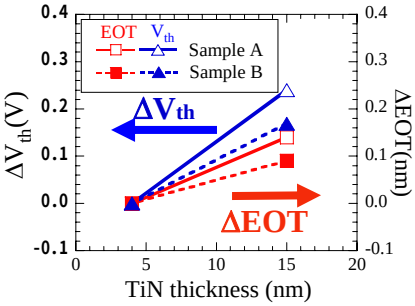


Fig.2 TiN thickness dependence of V_{th} and EOT with samples A and B.

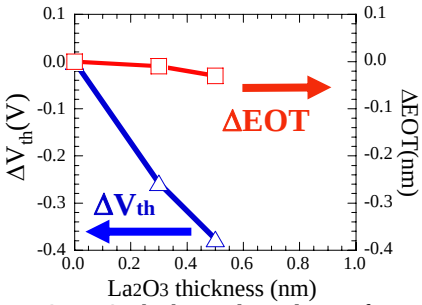


Fig.3 La_2O_3 thickness dependence of V_{th} and EOT with samples C.

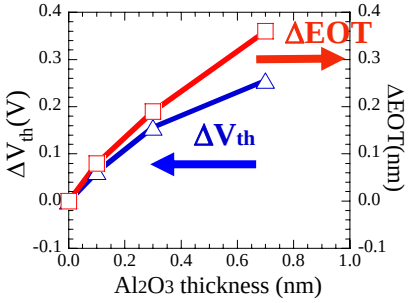
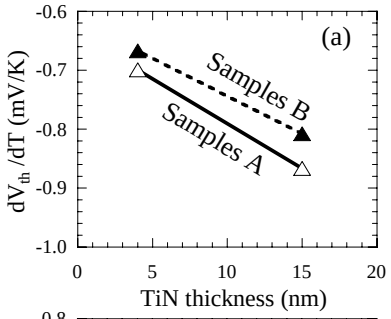
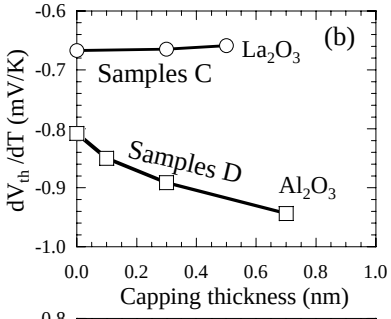
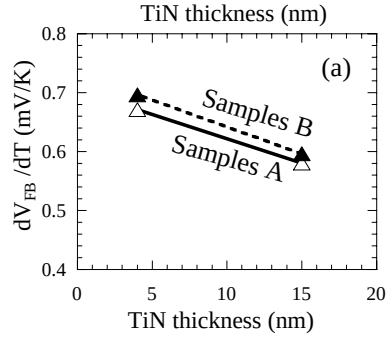


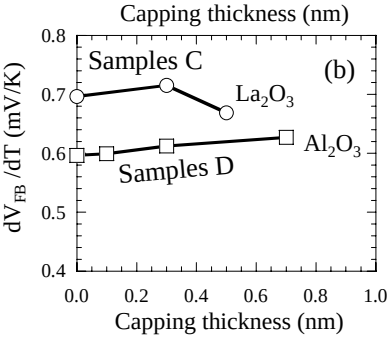
Fig.4 Al_2O_3 thickness dependence of V_{th} and EOT with samples D (nFET).



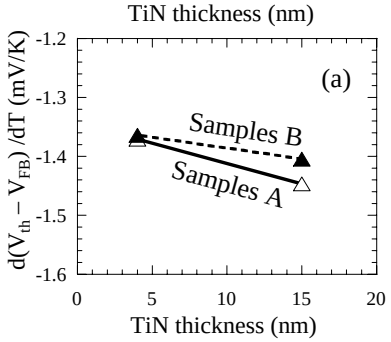


Figs.5
(a) TiN thickness dependence of dV_{th}/dT with samples A and B. Because dV_{th}/dT is negative value, a point which is at lower position in the graph means that V_{th} changes by large width during the temperature increases.
(b) La_2O_3 and Al_2O_3 capping thickness dependences of dV_{th}/dT with samples C and D.





Figs.6
(a) TiN thickness dependences of dV_{FB}/dT with samples A and B.
(b) Capping thickness dependences of dV_{FB}/dT with samples C and D.



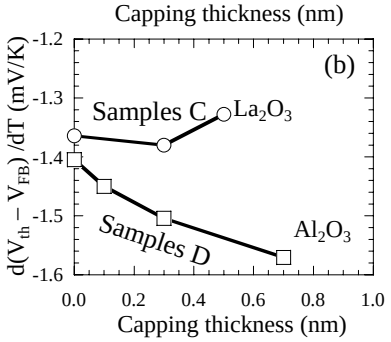


Fig.7 Characteristics of temperature coefficient of V_{th}–V_{FB}, which is the component affected by the third term of equation (1).
(a) TiN thickness dependences of $d(V_{th}–V_{FB})/dT$ with samples A and B.
(b) La_2O_3 and Al_2O_3 dependence of $d(V_{th}–V_{FB})/dT$ with samples C and D.

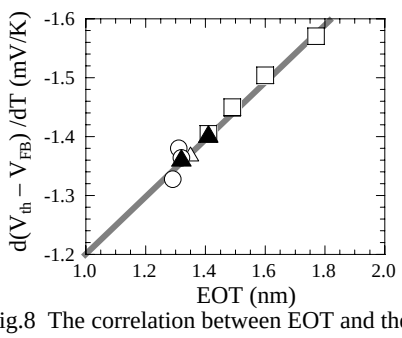


Fig.8 The correlation between EOT and the temperature coefficient of V_{th}–V_{FB} of all samples in this work. As expected from the third term of equation (1), $d(V_{th}–V_{FB})/dT$ is determined by $1/C_{ox}$, and decreased with the reduction of EOT.