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Impact of interface roughness on threshold-voltage variation in ultra-small three-dimensional MOSFETs

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1 Introduction

To overcome short channel effects in deep sub-100 nm conventional bulk-MOSFETs, several three-dimensional (3D) MOSFETs have been proposed, which include double-gate (DG) and gate-all-around (GAA) MOSFETs. The channel region in GAA MOSFETs is surrounded by the gate, while that in DG MOSFETs is sandwiched between the top and bottom gates. GAA MOSFETs are, therefore, expected to have better gate-control compared to DG MOSFETs. However, GAA MOSFETs are considered to show weaker tolerance to interface roughness because of stronger quantum confinement. To obtain quantitative understanding of this trade-off between gate-control and tolerance to interface roughness, we have performed 3D quantum-mechanical simulation of transport characteristics of DG and GAA MOSFETs.

2 Device Structure and Simulation Method

We consider n-type DG and GAA MOSFETs (see Fig. 1). For DG MOSFETs, the Si-body thickness is $t = 3$ nm or 4 nm and the gate width is $W = 2t$. For GAA MOSFETs, the Si quantum wire has a square cross section of $t \times t$ with $t = 3$ nm or 4 nm. Both devices have the same SiO_2 thicknesses of $t_{ox} = 0.8$ nm. The gate length, L_g, is varied from 5 nm to 12 nm.

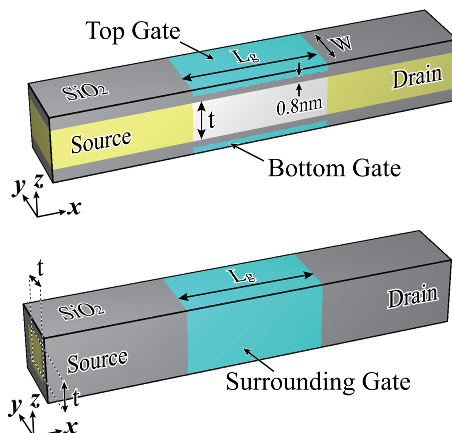

Figure 1: Schematic diagrams of DG (top) and GAA MOSFET (bottom) together with the coordinate system.

We used the non-equilibrium Green's function (NEGF) method to calculate source-to-drain current. The coupled eigen-mode expansion method [1, 2] is adopted for solving the NEGF transport equation. The conduction band is expressed in terms of six elliptic valleys within an effective mass approximation. We use the bulk effective masses in the present calculation. Interface roughness is generated between Si and SiO_2 interfaces using a Gaussian auto-correlation function.

3 Results and Discussion

Figs. 2 and 3 show the transfer characteristics of DG and GAA MOSFETs without interface roughness. For longer gate-lengths, both devices have similar characteristics except for V_{th} shift of $\approx$ 0.1 V. This shift is originated in the quantum confinement along the y-direction in the GAA MOSFET. The subthreshold swing of longer gate-length devices is very close to the ideal value of $(kT/q) \ln 10$. When the gate-length becomes shorter, the S-parameter increases. The GAA MOSFET achieves better gate control compared to the DG MOSFET (see Fig. 4).

Figs. 5 and 6 show the results with interface roughness. The average hight of the interface roughness is $\Delta = 0.2$ nm and the correlation length is $\Lambda = 2$ nm. We simulated 20 different interface-roughness patterns for each device structure. We find that V_{th} variation, ΔV_{th}, of GAA MOSFETs is almost two times larger than that of DG MOSFETs (see Fig. 7). By considering the fact that interface roughness affects not only the subband energy but also the transmission probability from source to drain, we obtain a simple analytical formula describing ΔV_{th} (dashed lines in Fig. 7).

[1] R. Venugopal, Z. Ren, S. Datta, and M.S. Lundstrom, *J. Appl. Phys.*, **92**, 3730 (2002).
[2] H. Takeda and N. Mori, *Jpn. J. Appl. Phys.*, **44**, 2664, (2005).

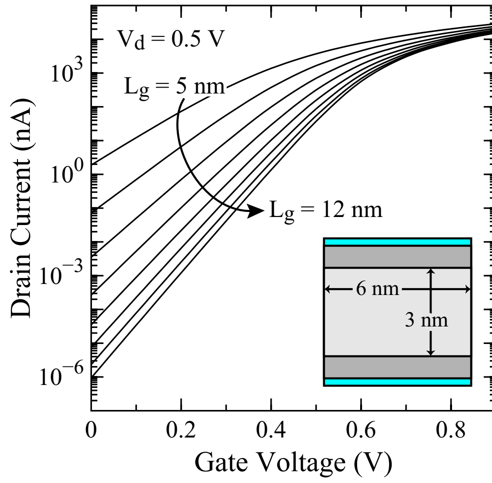

Figure 2: Drain-current–gate-voltage characteristics of DG MOSFET without interface roughness at V_d = 0.5 V and T = 300 K.

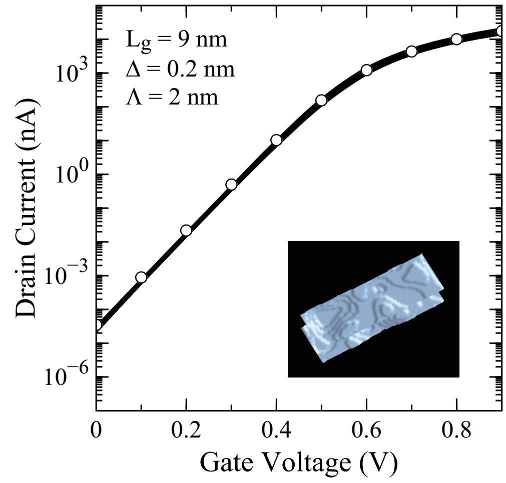

Figure 5: Drain-current–gate-voltage characteristics of DG MOSFET with (solid lines) and without (open circles) interface roughness.

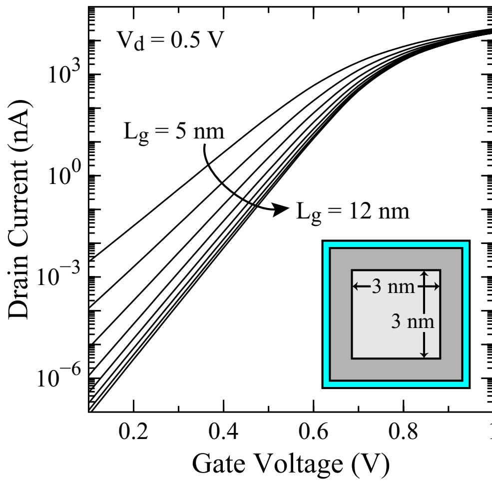

Figure 3: The same as Fig. 2 but for GAA MOSFETs.

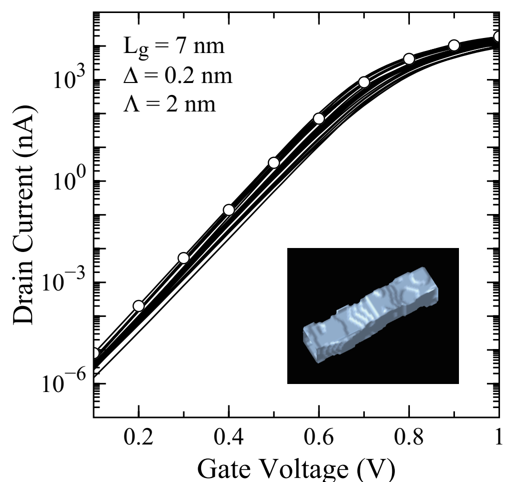

Figure 6: The same as Fig. 5 but for GAA MOSFETs.

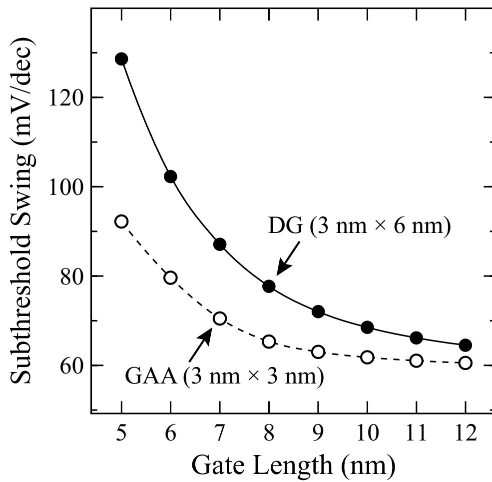

Figure 4: Gate-length dependence of subthreshold swing for DG (solid circles) and GAA (open circles) MOSFETs.

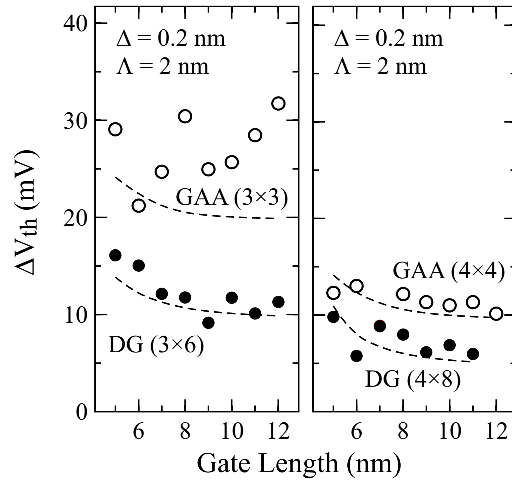

Figure 7: Gate-length dependence of threshold-voltage variation. Dashed lines shows the results of the compact model.