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Experimental Study on I_g RTS Noise of SiON/HfO_2/TaN PMOSFETs

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1. Introduction

When CMOS devices scale down to the 45nm node and beyond, the increasing of gate leakage current has brought high-k/metal gate stack technology on stage, which enables EOT continue reducing without a gate leakage current penalty. However, gate dielectric traps in these high-k stack devices are still a major concern. Probing and analyzing on gate current random telegraph signal (I_g RTS) noise has provided one sensitive tactic to investigate the physics-based properties of traps in SiO2 or SiON gate stack devices [1-5]. Very recently, some preliminary results of I_g RTS in high-k/metal gate stack devices have been reported [6]. However, further study is needed.

In this paper, further results and in-depth study on I_g RTS noise in SiON/HfO_2/TaN gate stack PMOSFETs are reported. Single carrier trapping/detrapping in the high-k/metal gate stack under NBTI stress is observed for the first time. The location of traps, the impacts of gate bias, temperature and substrate bias are discussed for understanding the RTS mechanism in high-k devices. Moreover, during long time stress, an abrupt change of amplitude of I_g fluctuation and the mean capture and emission time is also observed for the first time, which can be probably attributed to the slow trap or the generation of the new trap in HfO_2 layer.

2. Device structure and experiment

The device investigated in this work has a SiON/HfO_2/TaN/Poly-Si gate stack. The fabrication begins with the preparation of the 0.7nm interface oxide, followed by a nitridation ($6\times10^{14}cm^{-2}$). The 1.8nm HfO_2 layer is subsequently deposited as the high-k dielectric, and nitrogen annealing is performed to reduce EOT and improve its thermal stability. This process is followed by 100nm TaN deposition and subsequent poly-silicon deposition to form the gate electrode. Each device investigated in this work has a gate length of 100nm and a width of 10μm.

3. Results and discussion

The typical I_g RTS noise of p-type MOSFETs is illustrated in Fig. 1(a), which presents the I_g current fluctuation between two steady states, with fluctuation amplitude of 7.3%. The corresponding current power spectral density is illustrated in Fig.1(b), clearly showing Lorentzian spectrum $S_{Ig}(f)=A/(1+(f/f_c)^2)$. I_g RTS in HfO_2/TaN device can be attributed to the process that a single channel carrier is captured by the bulk trap (trap in the gate dielectrics) and then emitted to the TaN metal gate. When the charge is captured, it becomes an obstacle of the tunneling process and the gate current is accordingly reduced. Moreover, the capture (τ_c) and emission time (τ_e) in our work is defined corresponding to that of I_d RTS [7], as shown in Fig. 1(b). Besides the two-level RTS result, multi-level I_g RTS is also observed (Fig. 2), indicating co-impacts by several dielectric traps.

Important parameter of RTS, such as τ_c and τ_e are extracted under different gate voltages (Fig. 3). Both the decreasing τ_c and decreasing τ_e with increasing gate biases are observed, which is different from traditional I_d RTS that has uprising or constant τ_e. The capture kinetics in I_g RTS is described by the capture by a single trap within the gate dielectric. However, the captured carrier will be emitted to the TaN gate, but not back to the channel, which is the key difference between I_g RTS and I_d RTS. As a result, according to Shockley-Read-Hall (SRH) theory and the multi-phonon theory [8-9], the emission kinetics is affected and the equation for emission can be deduced as

$$\frac{1}{\tau_e} = c_n n \cdot \exp\left(\frac{E_T - E_V}{2kT}\right)\exp\left(\frac{E_{F(G)} - E_T}{kT}\right)$$

where c_n is the capture coefficient, n the density of carriers, E_T and $E_{F(G)}$ are the energy level of traps and Fermi level at the TaN gate. When $|V_g|$ increases, there will be an increase on both n and , $E_{F(G)} - E_T$ thus a reduction on τ_e can be obtained. The depth of the trap is extracted though [10], and its lateral location is investigated by applying forward and backward drain biases (Fig. 4). Results indicate that the corresponding traps are in the SiON interfacial layer and close to the drain side.

τ_c and τ_e at different temperatures under high-field and low-field stress were recorded in Fig. 5(a)(b). Both τ_c and τ_e show $\tau=\tau_{0*}\exp(B/T)$, where τ_0 and B (B>0) are fitting parameters, T the absolute temperature. The change of τ_c and τ_e can be caused by both carrier concentration variation and thermal activation of traps. In our experiment, the change of I_g under different temperature is small (not shown here), and the variation of τ_c and τ_e is mainly caused by thermal activation of bulk traps. Fig. 6 presents the impacts of substrate biases, which helps to further investigate the capture/emission kinetics. The substrate bias (V_b) will adjust the concentration of the inversion carriers (N_{inv}) and the capture kinetics is affected by the amount of available carriers according to the SRH theory. As a result, when $V_b<0$, which can cause an increase of N_{inv} for P-type FETs, the channel carrier is easier to be captured, and τ_c therefore decreases. Similar case occurs for the applied positive bias. In addition, τ_e is impacted by the Coulomb interaction between the inversion carriers and trapped holes, which causes the substrate bias dependence shown in Fig. 6.

In our experiments, I_g RTS keep constant as least for several thousands of seconds. However, for long time stress, we also observed an abrupt change on I_g RTS (Fig. 7). As discussed above, the trap causing Ig RTS probably exists in the SiON interfacial layer, in which new trap-related phenomenon may be brought in. This abrupt change can be divided into two types. Type one is that only the amplitude of I_g fluctuation changes while τ_c and τ_e keep almost constant (Fig. 7(a)(b)). As shown in Fig. 8(a), there may be a micro-system containing a fast trap and an adjacent slow trap, and each has a TAT channel. The hole trapped in the fast trap can block both TAT channels, while the hole trapped in the slow trap only block its own TAT channel. At beginning, the slow trap is empty and only the effect of the fast trap is observed. With stress time increases, a hole is trapped in the slow trap and the trapping/detrapping of the fast trap still exists, so that the fluctuation amplitude diminished but τ_c and τ_e does not changed a lot. Type two of the abrupt change is that only τ_c and τ_e varies while the amplitude of I_g fluctuation is still the same (Fig. 7(c)(d)). This may be attributed to the generation of a single trap under stress, as shown in Fig. 8(b). The capture and emission process is proceeding with the new generated trap that has a different cross-section and/or energy, which causes the change of τ_c and τ_e. Noticing that the minimum of I_g in phase two is a little lower than the maximum of I_g in phase one, thus there should be an interaction between the new generated trap and the original trap. More work is expected to investigate this unusual phenomenon in details.

3. Conclusions

In this paper, I_g RTS noise is studied in high-k PMOSFETs with SiO_2/HfO_2/TaN structure. The dependence of I_g RTS on the gate bias, temperature and substrate bias and trap locations are discussed. In addition, an abrupt change of I_g RTS during long time stress is reported for the first time, which can be probably attributed to the trapping of slow trap or generation of a new trap under stress in HfO_2 layer.

References: [1] N. Tega et al., *IEDM Tech. Dig.*, session 18.4, 2006; [2] L. Zhang et al., *Symp. on VLSI Tech. Dig.*, 3B-1, 2009; [3] H. H. Mueller et al., *J. Appl. Phys.*, p. 1734, 1998; [4] M.-J. Chen et al., *J. Appl. Phys.*, vol. 103, no. 3, 2008; [5] S. Kobayashi et al *Symp. on VLSI Tech. Dig.*, p.78, 2008; [6] C. M. Chang et al., *IEDM Tech. Dig.*, p.789, 2008; [7] Lode K. J. Vandamme et al., *IEEE Tran. Electron Devices*, vol. 55, p. 3070, 2008; [8] Mark Isler er al., *Phys. Rev. B.*, vol. 61, p. 7483, 2000; [9] A. Avellan et al., *J. Appl. Phys.*, vol. 94, p. 703, 2003; [10] K. K. Huang et al., *IEEE EDL*, Vol. 11, p. 90, 1990.

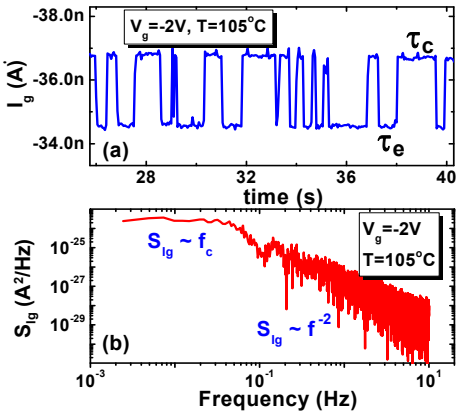

Fig.1(a) The typical I_g RTS noise of p-type MOSFETs and the corresponding current power spectral density, clearly showing Lorentzian spectrum $S_{Ig}(f)=A/(1+(f/f_c)^2)$.

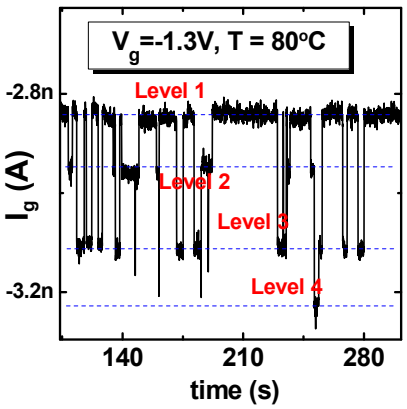

Fig.2 Four-level I_g RTS is also observed, indicating that the gate current is impacted by several dielectric traps. The multi-level Ig RTS is observed at V_g=-1.3V and T=80°C.

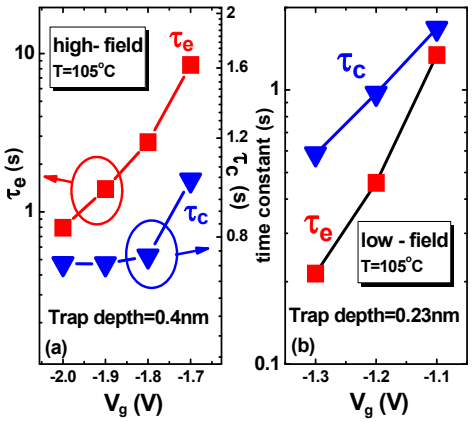

Fig.3 Extracted τ_c and τ_e under high-field stress and low-field stress. Both the decreasing τ_c and decreasing τ_e with increasing gate biases are observed.

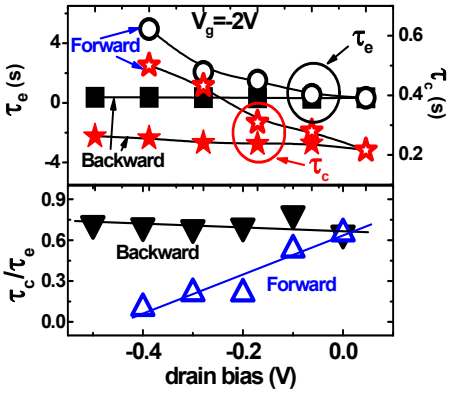

Fig.4 Extracted τ_c, τ_e and τ_c/τ_e under different forward and backward drain bias. The results indicate that the corresponding traps in the gate stack are close to the drain side.

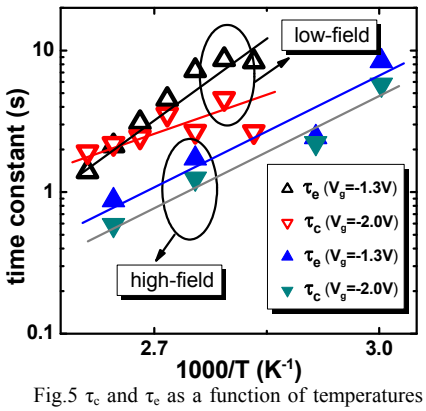

Fig.5 τ_c and τ_e as a function of temperatures at high-field (a) and low-field stress (b). Both τ_c and τ_e show $\tau=\tau_0*\exp(B/T)$, where τ_0 and B (B>0) are fitting parameters, T the absolute temperature.

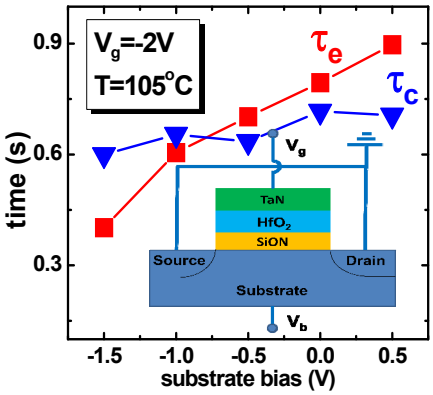

Fig.6 τ_c and τ_e as a function of substrate biases. The substrate bias (V_{bs}) will adjust the concentration of the inversion carriers (N_{inv}) and the capture/emission kinetics is affected.

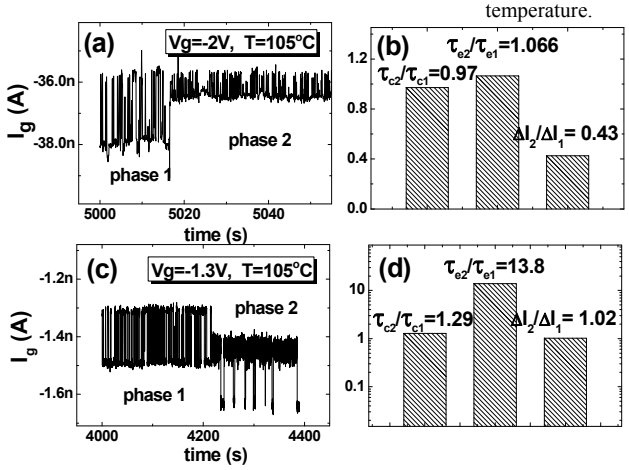

Fig.7 (a) (b) The first type of abrupt change of Ig RTS. Only the amplitude of I_g fluctuation changes while τ_c and τ_e keep almost constant; (c) (d) The second type of abrupt change of Ig RTS. Only τ_c and τ_e varies while the amplitude of I_g fluctuation is still the same.

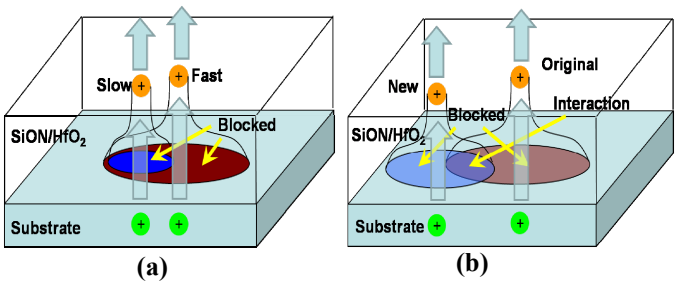

Fig.8 Illustration of the mechanism of the two abrupt change of I_g RTS. (a) There is a micro-system containing a fast trap and an adjacent slow trap, and each has a TAT channel. The hole trapped in the fast trap can block both TAT channels, while the hole trapped in the slow trap only block its own TAT channel. At beginning, the slow trap is empty, with stress time increases, a hole is trapped in the slow trap and the trapping/detrapping of the fast trap still exists. (b) A new trap is generated, which has a different cross-section and/or energy, and causes the change of τ_c and τ_e. There should be an interaction between the new generated trap and the original trap.