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Leakage and Matching Optimization of SRAM-cells for Wireless Applications

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Abstract

This paper presents SRAM key process steps to manage wireless and mobile applications in 65 & 45nm technologies. Based on a standard logic process flow, specific devices and layout optimisations provide ultra low leakage embedded SRAM. These techniques are fully scalable down to 32/28nm.

Introduction

Growing complexity and demand for mobile phone and multimedia handset are pushing chipmakers to reach better logic performance and to increase the amount of embedded SRAM memory (Fig.1,2) from node to node. At the same time, in order to extend battery life, static and dynamic power have to be reduced as much as possible. Nevertheless, due to increasing device spread from node to node, it is more and more difficult to fulfil products requirements, especially in the SRAM arrays that are major contributors in terms of power dissipation. Regarding static power, SRAM must exhibit the lowest stand-by leakage as possible. Fig. 3 shows the evolution of standby leakage I_{sb} from 130nm to 65nm node with classical processes. The leakage is increasing continuously, and innovative (but cost effective) solutions had to be implemented for the 65/55nm and 45/40nm nodes. Regarding the dynamic power reduction, chips using ultra low-power techniques such as Adaptative Voltage Scaling (AVS) and Adaptative Body-Bias (ABB) are gaining an enormous momentum [1]. In order to be effective, SRAM must be operating in the range $V_{dd} \pm 20\%$ and requires enhanced matching at the bit-cell level. In a first part we will detail a cost effective process optimization allowing ultra-low leakage SRAM at the 65/55nm node and how by relaxing layout on some bit-cells, leakage and performances can be improved compared to previous generation. In a second part we will discuss the extendibility and improvement of process robustness and variability at the 45nm node.

SRAM Stand-by leakage Optimization Techniques

The classical way used to reduce the sub-threshold current of SRAM MOS transistors consists in using an additional implantation before the gate deposition (VTNcell), which is additive with the one used in logic areas, to increase the transistor V_{th}. The main drawback of this process flow is an increase of junction leakage and consequently a degradation of stand-by current. We start with 65nm data to demonstrate the mechanism of optimization, since at this node the gate leakage is negligible. The dependency of I_{off} (at drain side) on nFET to the implanted dose in the channel is plotted in Fig. 4. It is clearly seen that I_{off} tends to saturate at high boron dose. Indeed, when a too important number of dopants are implanted in the channel, the Gate Induced Drain Lowering (GIDL) in the drain area, but also the surface S/D junction leakage component are increasing and are becoming superior to the thermal leakage. The surface component is essentially attributed to "un-useful" dopants that do not participate to the V_{th} control. Use of this classical process architecture did not allow reaching ITRS 65nm Isb requirements [2]. This problem can be solved by suppressing the SRAM V_{th} implant, and increasing the tilt angle of dedicated SRAM halo implantation (see process flow in Fig 5) above angles of 15-30° (see Fig.6 and Fig.7). The main advantage is a better localization of dopants in the channel below the gate (more efficiency for Vt control), and therefore a reduction of doping level for same transistor V_{th}. This technique is applicable in dense area with regular poly-pitched structures, such as SRAM, where angles can be tilted up to 45-55°. These values are well above the previously reported techniques [3,4]. By this way, gate natural shadow cover a large part of active area, resulting into a far less number of boron dopants in Source/Drain area. As a result, the S/D surface leakage component is dramatically reduced (Fig.8), without degrading yield (see Fig. 9). For the 65nm node 0.525µm² HVT bitcell, I_{sb} was reduced by ~1 decade, from 30pA/bit down to 4pA/bit. Fig.10 shows that only the junction leakage component is reduced by tuning the pocket dose and energy. Fig.8 evidences that even if S/D leakage is suppressed, GIDL remains a limiting point regarding halo implant dose.

Another technique consists in increasing gate lengths in order to make negligible the channel leakage component. For an increment of 20nm in 65nm technology, the area cost is less than 6% compared to 0.525um² bit cell (SRAM area is then increased to 0.56µm²), but a significant gain in Process-Voltage-Temperature (PVT) corners is then achieved. Using the halo engineering mentioned previously, we show in fig.11 that the total standby leakage is then reduced by a factor of 2 at room temperature and up to a factor of 5 at high temperature. Indeed, because gate and junction leakages do not vary as much as sub-threshold current with temperature and gate critical dimension, a huge gain in stand-by consumption is measured (see Fig.12). Fig.13 evidences that very low consumptions are obtained in PVT corners, with lower values than 2 technology nodes before (see Fig.3).

Extendibility to 45/40nm node : variability improvement and junction robustness

At the 45/40nm node halo optimization technique is also used, but its effect on S/D surfaces leakage component is found to be screened by the gate leakage component which becomes more important. Nevertheless, Fig. 14 shows that in the case of a low tilt pocket scheme, the electric field spatial extension goes far below SD-extension. In the case of local process variation, such as NiSi spiking, this drives to a strong increase of extrinsic leakage [5]. Highly tilted halos allow moving away the peak electric field from the spacer edge region and improve junction robustness. This is clearly evidenced in Fig. 15 where I_{sb} outlayers (coming from extrinsic leakages) are removed with high tilted pockets.

In addition, the reduction of effective dopant dose by halo optimization allows introducing co-implanted heavy ions like indium without Gidl penalty. It improves even further the doping efficiency and consequently the matching of SRAM transistors (σVt). A direct impact is a huge V_{min} improvement [6].

At the 32nm node, introduction of High-K/Metal gate is making again the junction leakage and GIDL the limiting component of stand-by leakage in SRAM, making the optimization of tilted halos and increase gate length powerful techniques to design ultra low leakage products.

Conclusion

We detailed cost efficient process optimization to obtain ultra low leakage SRAM bit cells for wireless applications, at the 65nm and 45nm nodes. Replacement of SRAM V_{th} adjust by highly tilted halos is beneficial to the reduction of junction leakage without change in Vth, and to the improvement of matching of transistor. This enables to use AVS or ABB design techniques to mitigate static power consumption.

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[4] J.-G.Su et al., Proc. Of Elect. Dev. Meeting, pp. 11-14, 2007
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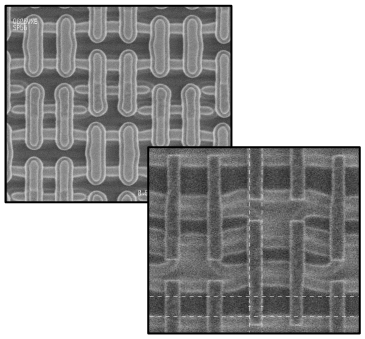

Fig.1 : SEM top-view of 0.525um² and 0.299µm² SRAM bitcell

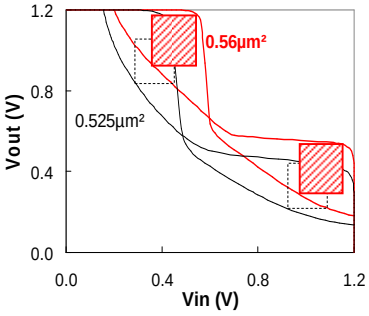

Fig.2 : Typical butterfly curves of bit-cells discussed in this paper.

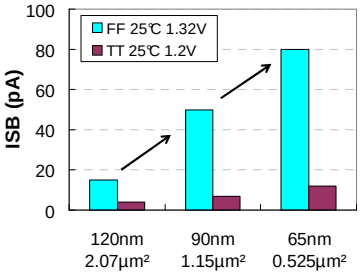

Fig.3 : I_{sb} of High-Density SRAM bitcells (with VTNcell implant before gate deposition)

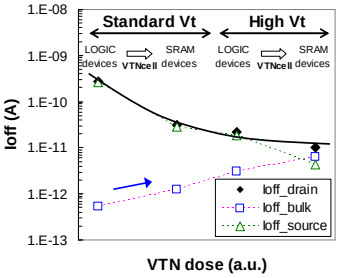

Fig.4: NMOS leakages for various channel doping level (with VTNcell implant before gate deposition)

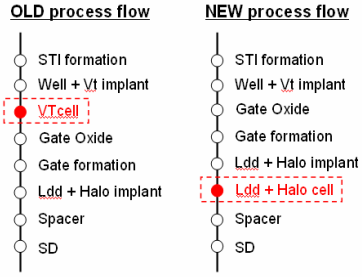

Fig.5 : Process flow change for SRAM specific implants

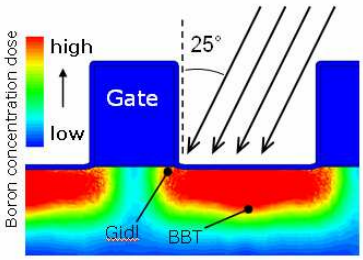

Fig.6 : Implant scheme with low angle halos that not use gate shadowing, driving to high Gidl and S/D diode leakages

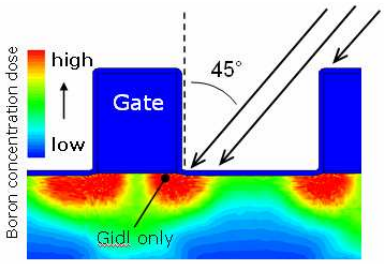

Fig.7 : Implant scheme with high tilted halos that use the natural gate shadowing. In that case, S/D surfacic diode leakage is suppressed.

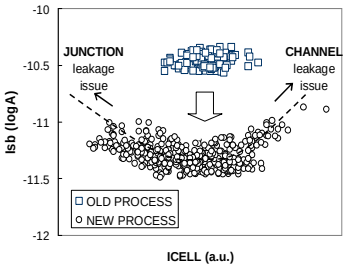

Fig.8 : Isb=f(Icell) for OLD ans NEW process

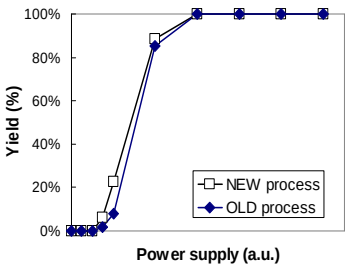

Fig.9 : Yield at various Vdd power supply for OLD and NEW process

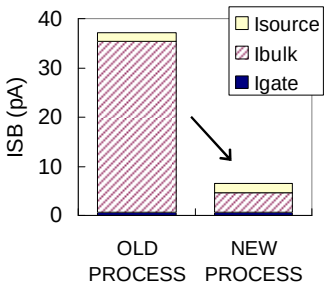

Fig.10 : Comparison of Isb leakage components between old and new process flow in 65nm.

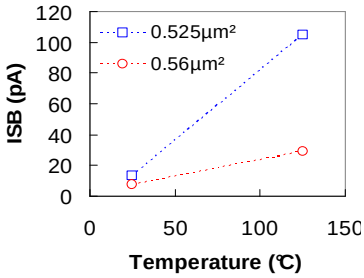

Fig.11 : Isb at 25 and 125°C for 0.525um² "Moore's like" bitcell and 0.56um² "Large L" bitcell

Bitcell leakages (pA)		25℃	125℃	Temp. ratio
0.56µm²	Isb	2.1	**28.9**	x14
	Isb_gate	0.8	8.0	x10
	Isb_junction	1.0	3.9	x4
	Isb_source	0.3	17.0	x57
0.525µm²	ISB	5.7	**105.7**	x19
	Isb_gate	0.7	6.5	x10
	Isb_junction	3.6	10.9	x3
	Isb_source	1.4	88.2	x63

Fig.12 : Isb leakage components for 0.525um² and 0.56um² bitcells at room and high temperatures

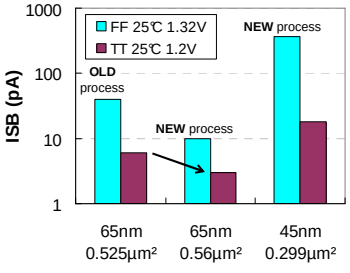

Fig.13 : Isb of bitcells studied in this work in typical (TT) and process (FF) corners

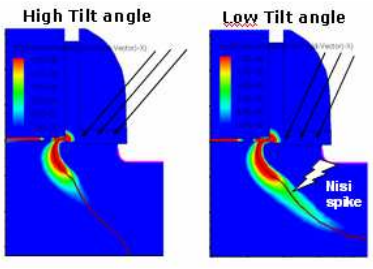

Fig.14 : 2D TCAD simulations showing electric field at drain side for high (left) and low (right) tilt angles

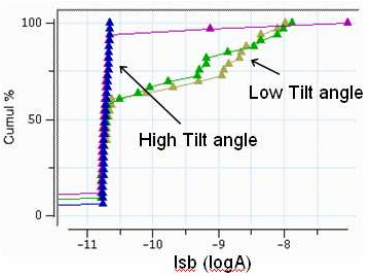

Fig.15 : Isb measurements showing huge reduction of extrinsic leakages with high tilted pockets