Stress variability control by defects suppression of SiGe Source/Drain using novel SiGe epitaxial growth technique

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Abstract

We found that pits near the recessed Si side wall of pMOSFETs with eSiGe degrade the device variability due to local tensile strain induced in the channel region. This was improved by newly developed SiGe epitaxial growth technique that includes two-step sequences with different amount of additional HCl in SiH₄-GeH₄-BH₃-HCl-H₂ gas mixtures. By using this technique, we achieved saturation drain current ($I_{DS}$) increase (4%) and improvement both in $L_{on}$ and threshold voltage variability.

1. Introduction

The strain enhancement technique with embedded silicon germanium (eSiGe) in the sourcetrain (SD) regions [1] has been matured, and therefore the demands for variability control and yield improvement have been strongly required. One of the most important keys is to suppress SiGe defects, because they seem to have the impact on device performance. Thus, such defects and the impacts should be studied, but they have not completely clarified yet. We have already reported that lowering temperature of SiGe growth can suppress the strain relaxation during SiGe growth and its effectiveness in CMOS process [2]. We also reported that the impact of SiGe/Si interfacial contamination on the dislocations and device performance [3].

In this work, we found another defect mode of “pit”. Pits are defined as the defects, where SiGe growth is locally suppressed near the recessed Si side wall (Fig. 1). We present newly proposed SiGe selective epitaxial growth (SEG) technique with SiH₄-GeH₄-BH₃-HCl-H₂ gas mixture for suppression of pits, and also present its effectiveness for the variability and device performance.

2. Variability degradation caused by SiGe defects

pFETs were fabricated by using our previous reported eSiGe process [4]. Figure 2 shows the distribution of $I_{on}$ of pFETs, and the several abnormal values which are deviated from the normal distribution are found. The channel hole mobility is also degraded in a typical degraded device (Fig. 3). In such devices, pits are found at the both sides near the recessed Si side wall, and nickel silicide (NiSi) approaches to the lateral regions of the recessed Si side wall as shown in Fig. 4. It is also found that tensile strain along <022> direction is induced to the channel region in pFET with pits in spite of using eSiGe and compressive silicon nitride (SiN) layer as shown in Fig. 5. This suggests that NiSi near the recessed Si side wall compresses the Si lattice to the vertical direction, and leading tensile channel stress (Fig. 6) due to its difference in the coefficients of thermal expansion between NiSi and SiGe [5]. These results mean that the channel compressive strain is locally reduced in the pits region, and those random strain reduction leads to the yield degradation.

3. Newly proposed SEG growth technique

3.1. Influence of HCl on pits generation and selective growth

Pits are found to generate more in the more highly SEG condition with higher HCl partial pressure ($P_{HCl}$) as shown in Fig. 7. In such higher $P_{HCl}$ condition, the amount of residual Cl at the SiGe/Si interface is also larger, while Cl is not found inside the SiGe film (Fig. 8). SiGe growth is suppressed on the Cl-passivated Si surface (Fig. 9) as reported in our previous paper [6]. These results suggest that HCl adsorbs on Si surface more heavily in higher $P_{HCl}$ cond-

4. Conclusion

It is found that tensile strain is induced locally to the channel region of pFETs by pits. We propose newly developed SiGe selective epitaxial growth technique that includes two-step sequences with different amount of additional HCl. Pits can be suppressed by lowering HCl at initial stage of SiGe growth, and selective growth can be achieved by raising HCl at 2nd step. eSiGe device performance and its variability are improved by using this technique.

Reference

Fig. 1. (a) Plane-view and (b) cross-sectional SEM photographs of pFET gate.

Fig. 2. Distribution of normalized $I_m$ as a function of inversion carrier concentration.

Fig. 3. Effective hole mobility on the Cl pre-adsorbed Si surface.

Fig. 4. Cross-sectional TEM images of eSiGe (a) without pits and (b) with pits.

Fig. 5. Channel strain measured by nano beam diffraction analysis.

Fig. 6. Assumed model of NiSi stress to eSiGe with pits.

Fig. 7. SEM images of eSiGe grown with (a) high $P_{ACC}$ and (b) low $P_{ACC}$, and normalized pit density as a function of normalized $P_{ACC}$.

Fig. 8. SIMS profiles of Cl at SiGe/Si interface.

Fig. 9. Amount of Ge adhesion on the Cl pre-adsorbed Si surface by SiH$_4$, GeH$_4$, BiH$_3$, H$_2$.

Fig. 10. $P_{ACC}$ dependence of (a) SiGe thickness on Si as Sn, and (b) their incubation time.

Fig. 11. (a) Basic concept and (b) process sequence of newly proposed SiGe growth.

Fig. 12. Distribution of pits number in an active area. Active width is 1.0 μm.

Fig. 13. Leakage current between Gate and Source/Drain.

Fig. 14. Surface morphologies of (a) conventional SiGe and (b) proposed SiGe observed by AFM.

Fig. 15. Distribution of normalized $I_m$.

Fig. 16. Pelgrom plots of pFETs.