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Stress variability control by defects suppression of SiGe Source/Drain using novel SiGe epitaxial growth technique

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Abstract

We found that pits near the recessed Si side wall of pMOSFET with eSiGe degrade the device variability due to local tensile strain induced in the channel region. This was improved by newly developed SiGe epitaxial growth technique that includes two-step sequences with different amount of additional HCl in SiH_4-GeH_4-B_2H_6-HCl-H_2 gas mixtures. By using this technique, we achieved saturation drain current (I_{on}) increase (4%) and improvement both in I_{on} and threshold voltage variability.

1. Introduction

The strain enhancement technique with embedded silicon germanium (eSiGe) in the source/drain (SD) regions [1] has been matured, and therefore the demands for variability control and yield improvement have been strongly required. One of the most important keys is to suppress SiGe defects, because they seem to have the impact on device performance. Thus, such defects and the impacts should be studied, but they have not completely clarified yet. We have already reported that lowering temperature of SiGe growth can suppress the strain relaxation during SiGe growth and its effectiveness in CMOS process [2]. We also reported that the impact of SiGe/Si interfacial contamination on the dislocations and device performance [3].

In this work, we found another defect mode of "pit". Pits are defined as the defects, where SiGe growth is locally suppressed near the recessed Si side wall (Fig. 1). We present newly proposed SiGe selective epitaxial growth (SEG) technique with SiH_4-GeH_4-B_2H_6-HCl-H_2 gas mixture for suppression of pits, and also present its effectiveness for the variability and device performance.

2. Variability degradation caused by SiGe defects

pFETs were fabricated by using our previous reported eSiGe process [4]. Figure 2 shows the distribution of I_{on} of pFETs, and the several abnormal values which are deviated from the normal distribution are found. The channel hole mobility is also degraded in a typical degraded device (Fig. 3). In such devices, pits are found at the both sides near the recessed Si side wall, and nickel silicide (NiSi) approaches to the lateral regions of the recessed Si side wall as shown in Fig. 4. It is also found that tensile strain along <022> direction is induced to the channel region in pFET with pits in spite of using eSiGe and compressive silicon nitride (SiN) layer as shown in Fig. 5. This suggests that NiSi near the recessed Si side wall compresses the Si lattice to the vertical direction, and leading tensile channel stress (Fig. 6) due to its difference in the coefficients of thermal expansion between NiSi and SiGe [5]. These results mean that the channel compressive strain is locally reduced in the pits region, and those random strain reduction leads to the yield degradation.

3. Newly proposed SiGe growth technique

3.1. Influence of HCl on pits generation and selective growth

Pits are found to generate more in the more highly SEG condition with higher HCl partial pressure (P_{HCl}) as shown in Fig. 7. In such higher P_{HCl} condition, the amount of residual Cl at the SiGe/Si interface is also larger, while Cl is not found inside the SiGe film (Fig. 8). SiGe growth is suppressed on the Cl-passivated Si surface (Fig. 9) as reported in our previous paper [6]. These results suggest that HCl adsorbs on Si surface more heavily in higher P_{HCl} condition, and the adsorbed Cl suppresses the SiGe growth, and thus, leading to pits generation. In the recessed Si side wall, there should be much process damage such as side wall etching damage or halo ion implantation. On such surface, HCl adsorption may easily occur or Cl desorption may hardly occur. On the other hand, lowering P_{HCl} shortens the difference of incubation time (τ_{inc}) between SiGe growth on Si and that on SiN (Fig. 10), and as a result, selectivity breaking occurs on SiN. SiGe growth on the side wall SiN should be avoided, because this causes electrical short between gate and SD. Thus, these results indicate that pits suppression by lowering P_{HCl} is inconsistent with selective growth.

3.2. Newly proposed SEG technique

In order to suppress both pits and selectivity breaking, we propose newly developed SEG technique that includes two-step sequences with different conditions of P_{HCl} (Fig. 11). The growth sequence is explained as follows. At first, some SiGe seeds layer is formed with low P_{HCl} to suppress much Cl adsorption on Si surface, and then SiGe is grown up to the demanded thickness with high P_{HCl}. Selectivity breaking can be suppressed by growing each SiGe layer with in each τ_{inc}. Figure 12 compares the distributions of pits density. Proposed SEG is found to be effective for pits suppression, while the density of pits and each size of pit are various in a conventional method as shown in SEM image. Thus, the amount of strain degradation by pits (Fig. 4) may be varied according to their density or sizes. This suggests that pits causes the variability of stress effect, and degrade the variability of device performance, and as a result, degrade the yield.

SiGe over growth on the gate top is also suppressed with proposed method, leading to the improvement of leakage characteristics between gate and SD (Fig. 13). Misfit dislocations can also be suppressed as shown in Fig. 14. This is supposed due to the reduction of residual Cl in the SiGe/Si interface by the same mechanism as the SiGe/Si interfacial O and C [3]. Thus, this newly proposed method with two-step sequences is effective to suppress pits, misfit dislocations, and SiGe over growth on the gate top.

Variability of I_{on} is improved and abnormal values which are deviated from the normal distribution are eliminated by suppressing pits with proposed SEG (Fig. 15). The median value of I_{on} is also improved by 4%, and this is supposed due to the improvement of stress effect by suppressing dislocations. Further, the variability of threshold voltage is also improved (Fig. 16) by suppression of the stress variability by eliminating pits. Thus, it is found that device performance and its variability can be improved by using proposed SEG.

4. Conclusion

It is found that tensile strain is induced locally to the channel region of pFETs by pits. We propose newly developed SiGe selective epitaxial growth technique that includes two-step sequences with different amount of additional HCl. Pits can be suppressed by lowering HCl at initial stage of SiGe growth, and selective growth can be achieved by raising HCl at 2nd step. eSiGe device performance and its variability are improved by using this technique.

Reference

[1] T. Ghani et al, IEDM Tech. Dig., p.978, 2003. [2] Y. Shimamune et al, VLSI Tech. Dig., p.116, 2007. [3] M. Fukuda et al, ECS Trans. **19**, 213 (2009). [4] T. Miyashita et al, IEDM Tech. Dig., p.251, 2007. [5] I. Peidous et al., ECS Trans., 16 (10), p.551, 2008. [6] Y. Shimamune et al, 4th int. workshop on new group IV semicon. nanoelectronics,, p.13, 2008.

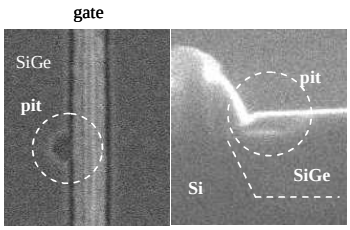

Fig.1. (a) Plane-view and (b) cross sectional SEM photographs of pFET

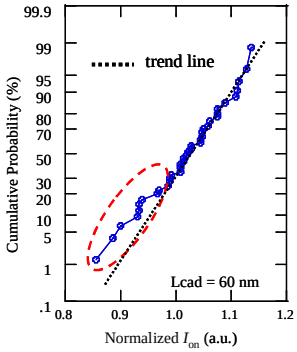

Fig.2. Distribution of normalized I_{on}.

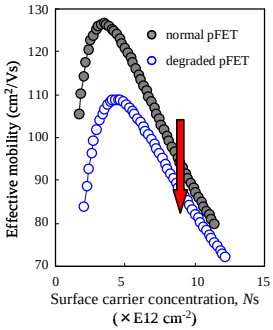

Fig.3. Effective hole mobility as a function of inversion carrier concentration.

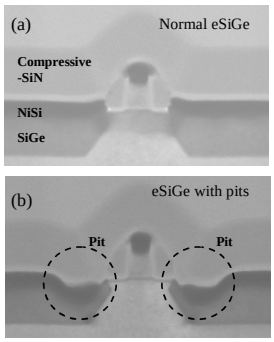

Fig.4. Cross sectional TEM images of eSiGe (a) without pits and (b) with pits.

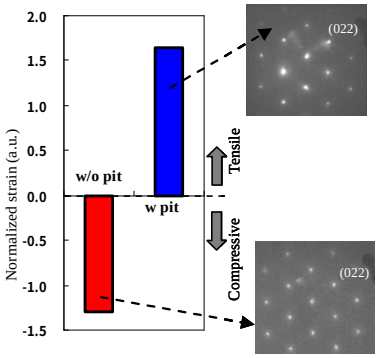

Fig.5. Channel strain measured by nano beam diffraction analysis.

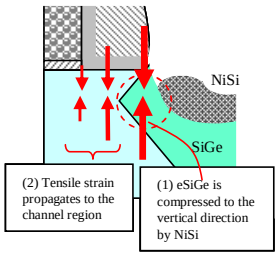

Fig.6. Assumed model of NiSi stress to eSiGe with pits.

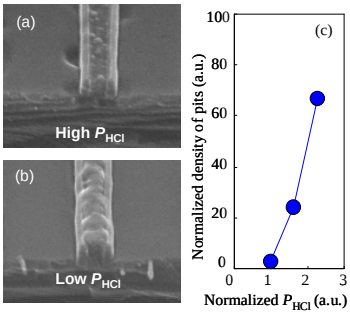

Fig.7. SEM images of eSiGe grown with (a) high P_{HCl} and (b) low P_{HCl}, and normalized pit density as a function of normalized P_{HCl}.

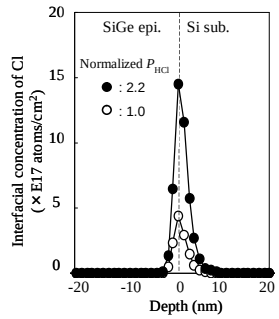

Fig.8. SIMS profiles of Cl at SiGe/Si interface.

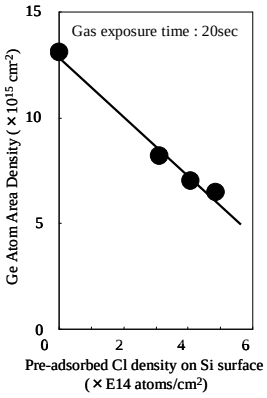

Fig.9. Amount of Ge adsorption on the Cl pre-adsorbed Si Surface by SiH_4-GeH_4-B_2H_6-H_2.

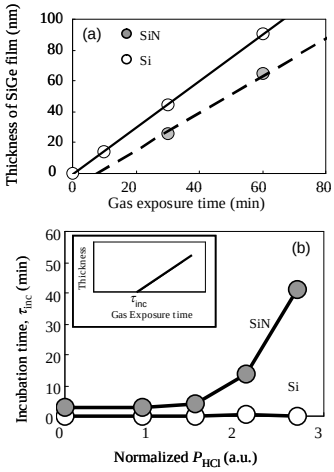

Fig.10. P_{HCl} dependence of (a) SiGe thickness on Si an SiN, and (b) their incubation time.

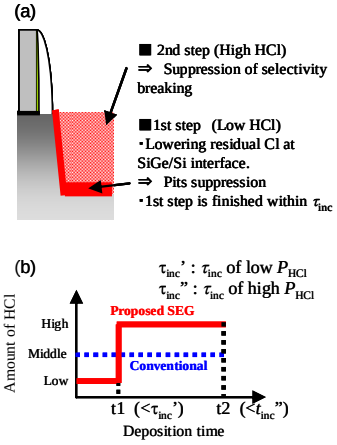

Fig.11. (a) Basic concept and (b) process sequence of newly proposed SiGe growth.

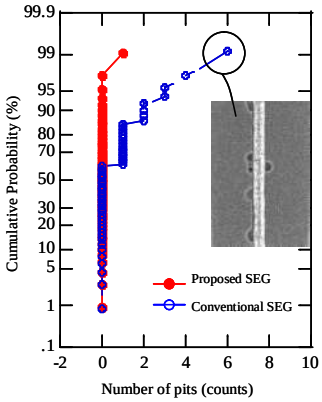

Fig.12. Distribution of pits number in an active area. Active width is 1.0 μm.

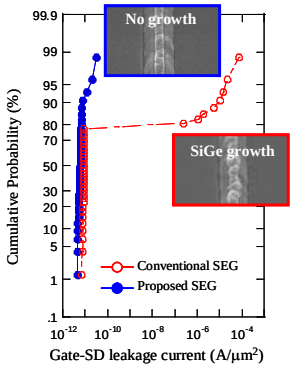

Fig.13. Leakage current between Gate and Source/Drain.

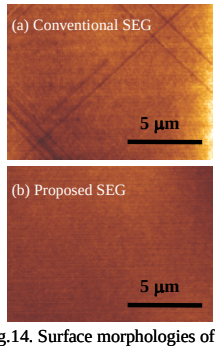

Fig.14. Surface morphologies of (a) conventional SiGe and (b) proposed SiGe observed by AFM.

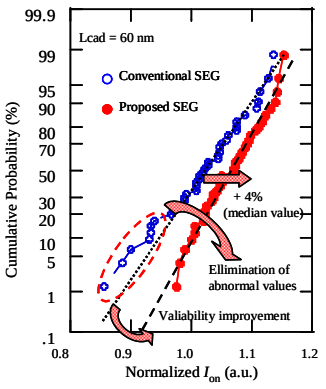

Fig.15. Distribution of normalized I_{on}.

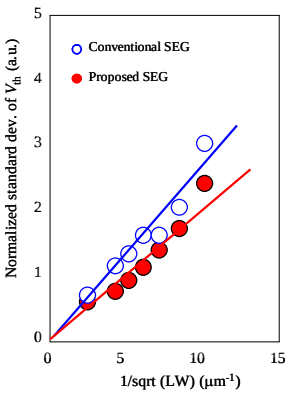

Fig.16. Pelgrom plots of pFETs.