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Multiple-Gate Tunneling Field Effect Transistors with sub-60mV/dec Subthreshold Slope

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Abstract

Complementary Multiple-Gate Tunneling Field Effect Transistors (MuGTFETs), implemented in a MuGFET technology [1] compatible with standard CMOS-processing, are fabricated and characterized. Measured devices show a point slope of 46mV/dec at low biases and an I_{on}/I_{off} ratio of 10^6 at a supply voltage of 1.2V. A dependence of the tunneling current on the fin width is reported and discussed for the first time. The impact of the gate length and temperature are also presented.

1. Introduction

As CMOS scaling is reaching fundamental limits, alternative approaches are being pursued. One of the most promising options consists of changing the operation principle of the device, through the use of Band-To-Band-Tunneling (BTBT) controlled by a gate [2]. This device has the potential of achieving sub-60mV/dec subthreshold slope and extremely low I_{off} because its carrier injection is no longer limited by carrier diffusion. In this paper we investigate the electrical characteristics of MuGTFETs, highlighting a fin width dependence.

2. Device fabrication

The TFET devices (gated P-i-N diodes) were fabricated on a (100) SOI substrate with 65nm thick Si film on top of a 145nm BOX. Fin widths down to 25nm were patterned using 193nm optical lithography and aggressive resist and hardmask (HM) trimming. The channel of the device was left undoped. The gate stack consists of a 100nm poly silicon layer on top of a 5nm MOCVD TiN layer, a high-k 2nm ALD HfO_2 on a 1nm interfacial oxide (Fig. 1). After gate patterning, complementary source/drain doping was obtained by an As/BF_2 extension implantation at 45° tilt parallel to the gate using a modified mask design (Fig. 2). Then, 50nm wide RTCVD nitride spacers were formed on a 5nm PECVD oxide liner. After HDD implantations, a 1050°C spike anneal was given followed by NiSi silicidation. No selective epitaxy was performed in the SD regions.

3. Results and discussion

N- and p-type tunneling currents are observed on the same device structure and the input characteristics are shown in figure 3. As shown in the figure, the side where the tunneling occurs is kept grounded. We notice that the device exhibits better performance in pTFET operation than nTFET, likely due to the sharper junction profile at the N+ side because of the lower diffusivity of arsenic used as n-type dopant, compared to boron at the P+ side. An I_{on}/I_{off} ratio of 10^6 at a V_{DD} of 1.2V is obtained for the pTFET operation. A minimum point slope of 46mV/dec is extracted at low bias (V_{GS}=0.2V, V_{DS}=-0.1V) for the 25nm wide fin device. This result is in line with previous reports of minimum point slope in planar TFETs which are also for very low bias [3][4].

MuGFETs are very attractive for CMOS technology because of their very good electrostatic control of the gate over the channel. In TFETs, the improved gate control over the channel potential is also expected to improve the tunneling current. For this reason we have investigated the impact of the fin width on the TFET characterictics. A plot of the ON current versus square root of the fin width clearly shows a sharp increase for fins below 80nm, where the two gates at the sidewalls of the fin become coupled to each other (Fig. 4). Comparing the $I_{DS}(V_{GS})$ characteristics of different devices, a reduction of the onset voltage of tunneling is observed for narrow fins (Fig. 5a). After normalization of the onset voltage, an increase of the tunneling current at large gate voltage is still visible (Fig. 5b). A possible dependence on the silicon body thickness was theoretically introduced for double-gate structures [5], [6] and is verified here for the first time. For narrow fins, there is a qualitative agreement with these models, which are based only on electrostatic calculations. However, the lack of quantitative agreement makes us suspect that differences in doping profile and/or interface trap density between the narrow and the wide fins need to be taken into account (Fig. 6).

The output characteristics in figure 7 show a perfect saturation of the device resulting in very low small-signal output conductance, making these devices very attractive for analog circuits. At low gate voltages an increase of the current is observed for large reverse bias, corresponding to an onset of tunneling at the opposite junction (Fig. 8).

No dependence on the gate length is observed (Fig. 9) down to 160nm. For very long channels, a slight decrease is observed due to the large resistance of the undoped channel. Figure 10 shows a very weak dependence of the tunneling current on the temperature, which is characteristic of tunneling. The OFF current shows an increase with the temperature proportional to the intrinsic carrier concentration, n_i, (Fig. 11) in line with the SRH generation current [7].

4. Conclusion

A minimum point slope of 46mV/dec is demonstrated for the first time in Multi-Gate Tunneling FETs. I_{on}/I_{off} ratio of 10^6 at V_{DD} of 1.2V in 25nm wide fin devices is reported. Tunneling dependence with fin width is shown experimentally. The combined effects of the improved gate control and the higher doping profile concentrations can explain the better performance of narrow fins compared to

the wide fins. No dependence on the gate length down to 160nm and a weak dependence with temperature make these devices attractive for further scaling and high temperature circuit operation.

Acknowledgements

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References

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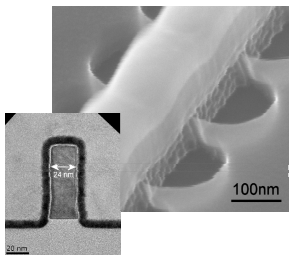

Fig. 1. SEM image after the gate patterning and High Resolution TEM (HRTEM) of a fabricated 25nm wide fin.

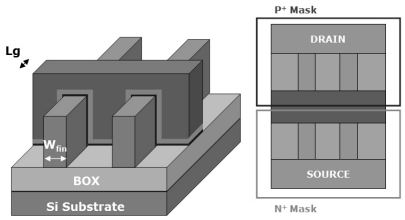

Fig. 2. Schematic view of the tunneling MuGFET structure and its implementation.

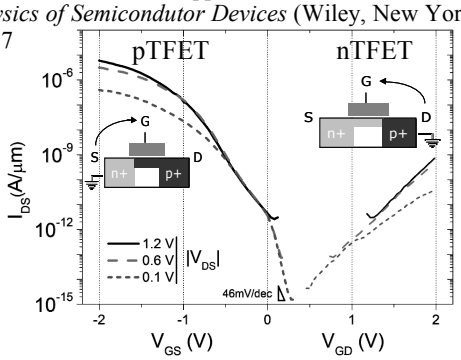

Fig. 3. pTFET and nTFET input characteristics for a 25nm wide fin (L_g=160nm).

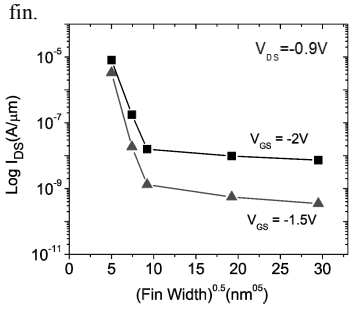

Fig. 4. W_{fin} dependence for different V_{GS} (L_g=160nm). Sharp increase of the tunneling current observed for narrow fins.

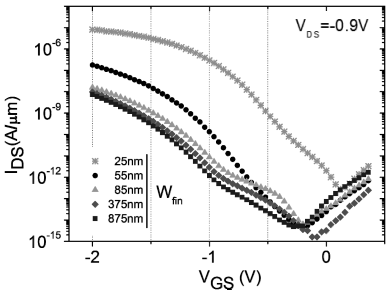

Fig. 5a. Original pTFET input characteristics for different fin width (L_g=160nm). Gate leakage dominates the characteristic of wide fins at low gate bias.

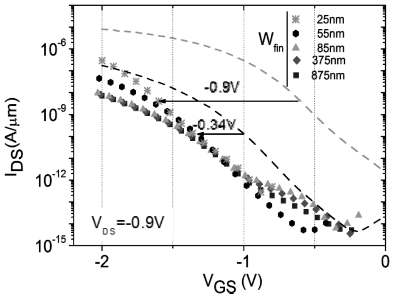

Fig. 5b. Shifted pTFET input characteristic for different fin width (L_g=160nm). The curves are shifted such that all the curves cross the data point of the 875nm wide fin. 25nm and 55nm original curves are shown with dashed lines to show the amount of shift of the tunneling onset.

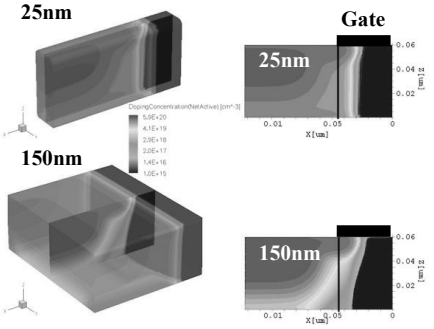

Fig. 6. TCAD simulated doping profile for a narrow fin (25nm wide) and a wide fin (150nm wide) after the HDD implantation. Only the silicon region is shown. The narrow fin benefits from the 45° tilt implant.

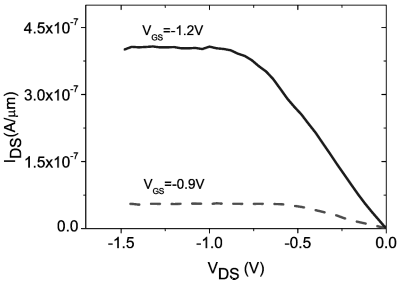

Fig. 7. I_{DS} vs V_{DS} for the 25nm wide fin (L_g=160nm).

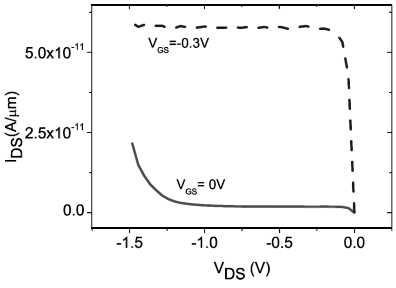

Fig. 8. I_{DS} vs V_{DS} for the 25nm wide fin for low gate voltages (L_g=160nm). Exponential increase of the drain current in the bottom curve represents the onset of tunneling at the drain side.

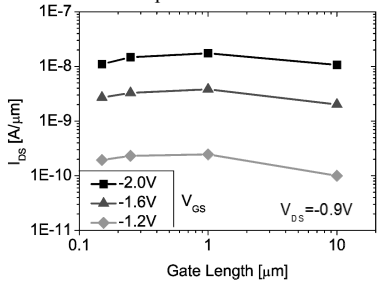

Fig. 9. Gate length dependence for 85nm wide fins.

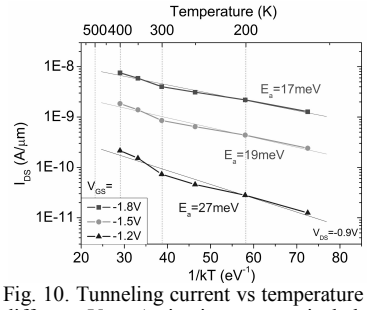

Fig. 10. Tunneling current vs temperature at different V_{GS}. Activation energy is below 30meV. (W_{fin}=85nm, L_g=160nm).

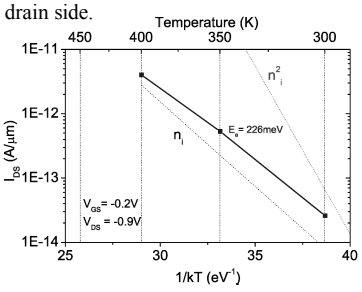

Fig. 11. I_{OFF} vs temperature. I_{OFF} is taken as the minimum value of the transfer characteristics of the device. Wfin is 85nm (L_g=160nm).