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NiSi metal S/D transistors with ultimately low Schottky barrier by sulfur implantation after silicidation process

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Abstract

The Schottky barrier height (SBH) for electrons at NiSi/Si lower than 10meV was realized through Sulfur Implantation After Silicidation (S-IAS) process [1]. S-IAS process was studied in detail and applied to NiSi source/drain Schottky barrier (SB) MOSFETs. It was found that the saturation is suppressed SB MOSFETs, which leads to higher drivability and better short channel effect immunity of S-IAS SB compared with those of conventional MOSFETs.

Introduction

Metal source/drain SB MOSFET has attracted much attention as a candidate of the future high-performance device beyond 22nm generation due to its ideally abrupt and shallow junctions etc [2]. The most serious issue for realizing SB MOSFETs is Schottky barrier at the interface of metal electrode and silicon. It was reported that S and selenium at the interface of NiSi electrode and Si reduced the SBH for electrons from 650meV to 70meV [3] and to 120meV [4], respectively. In these works, S and Se were introduced at the interface through Implantation Before Silicidation (IBS) process, in which impurities are implanted into Si prior to Ni silicidation. However, the SBH lower than the room temperature ~30meV is necessary for realistic operation of SB MOSFETs.

We have succeeded in SBH reduction lower than 10meV through S-IAS process [1], in which S is implanted after Ni silicidation [5]. In this paper, we study the details of S-IAS process and apply this technique to NiSi source/drain SB MOSFETs. The characteristics of this SB MOSFET are discussed in comparison with those of the conventional one.

S-IAS Process

The process flow and concept of IAS process are shown in Fig.1. S ions are implanted into a 16nm layer of NiSi with 5% Pt (NiPtSi) at 10keV. Since the projection range of S at 10keV is 8nm, most of the S ions are implanted inside of NiPtSi. S ions diffuse in NiPtSi during drive-in annealing, and trapped in the potential valley at the interface of NiPtSi/Si. This dynamics can be seen in Fig.2, which shows S profiles around the interface before and after drive-in annealing measured by atom probe technique. The horizontal axis is the distance from the interface along the direction perpendicular to the interface and hence the broadness of the profile arising from the roughness of the interface is eliminated. A sharp peak of S at the interface appearing after drive-in annealing indicates that S atoms are trapped at the interface during the heat treatment. The *IV*-characteristics of NiPtSi/Si diodes in Fig.3 also show the role of the drive-in annealing. The reverse current becomes larger after annealing, because implanted S atoms are accumulated and are activated at the interface. Note that the forward current before annealing is smaller than that after annealing that is almost the same as that of the reference, indicating that the NiPtSi/Si junction damaged by the implantation is recovered through heat treatment. This is confirmed by the TEM image in Fig.4, where no damage can be observed in spite of the high S dose of $1x10^{15}cm^{-2}$. Fig.5 shows the annealing temperature dependence of the reverse current modulation. As the temperature becomes higher, the reverse current becomes larger due to SBH reduction, and finally reaches the saturation. Our results through IAS process are summarized in Fig. 6. IAS process reduces SBH more than IBS in both S and Se cases. The implantation energy for Se was 15keV such that the projection range would be 8nm. The SBH by S-IAS (<10meV) is lower than that by Se-IAS (60meV). At this moment, S-IAS is the only way to achieve the NiSi/Si SBH lower than the room temperature 30meV. S-IAS process is applied to NiSi/Si (without Pt) and PtSi/Si diodes as well as NiPtSi/Si. Although the initial SBHs (without S doping) are quite different, the modulated SBHs are similar as shown in Fig.7. This implies that S atom pins the Fermi level near the conduction band edge regardless of the sort of the silicide.

Application to SB MOSFETs

The I_d-V_g characteristics (V_d=0.1V) of NiSi source/drain SB n-MOSFETs with S-IAS process at the dose of zero, $1x10^{14}$ and $1x10^{15}$ cm^{-2} are shown in Fig.8. The on-current increases as the S implantation dose becomes higher whereas the off-leakage suppression can be seen in the S-doped samples. This reflects that the SBHs for electrons and holes modulate in opposite directions. The I_d-V_g of $ErSi_2$ SB MOSFET is also plotted in Fig.8. $ErSi_2$ is one of the most studied metals for the electrode material of SB n-MOSFET because $ErSi_2$/Si has relatively low SBH of 0.3eV. It is clear that our S-IAS NiSi shows better performance than $ErSi_2$.

The I_d-V_d characteristics of SB with S-IAS process are compared with those of a conventional in Fig.9. I_d of the SB is almost the same as that of the conventional in the small V_d region, indicating that the parasitic resistance in the SB MOSFET is sufficiently lowered by S-IAS process. However, I_d of the SB becomes much larger than that of the conventional in the saturation region. This can be explained by the difference between the metal/Si and conventional pn junctions at the drain edge. The band bending at the metal/Si junction can be infinitely sharp while that at the pn junction is smooth. Therefore in the SB case, the electric field from the drain is terminated at the junction and does not penetrate into the channel as deeply as in the conventional case, as shown in Fig.10. This suppresses the saturation of SB MOSFET, resulting in the larger drive current as long as SBH is sufficiently low. This hypothesis can be supported by Fig.11 in which V_{th} is not sensitive to V_d for SB MOSFET while it drops drastically where V_d >1.5V for conventional one. This result indicates that the electric field penetration from the drain is smaller for SB than conventional MOSFET. This character of SB MOSFETs can suppress the short channel effect and enhance the drive current when the SBH is sufficiently low.

Conclusion

It has been experimentally shown that S-IAS process is a reasonable process to reduce the SBH of Ni(Pt)Si/Si sufficiently for realizing SB-MOSFETs. We applied this process to SB MOSFETs and showed that SB device with S-IAS process can have better performance than conventional ones from the viewpoint of both current drivability and short channel immunity. Therefore, SB MOSFET by S-IAS process is promising as sub-20nm device.

References

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[3] Q. T. Zhao, et al., Appl. Phys. Lett. **86**, 062018 (2006).
[4] H.-S. Wong, *et al*., IEEE Elec. Dev. Lett. **28**, 1102 (2007).
[5] Y.-C.Yang, presented in MRS 2009

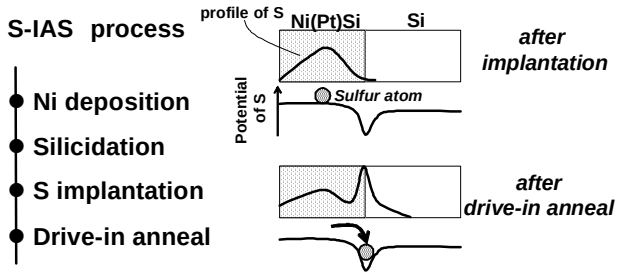

Fig.1: Process flow and principle of S-IAS process.

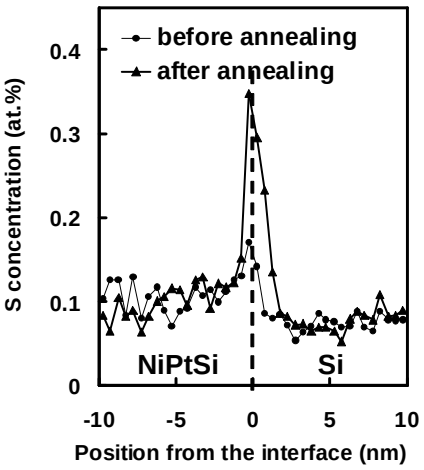

Fig.2: S profiles by atom probe analysis before and after drive-in annealing at 450°C for 1min. S implantation dose is $1x10^{15}$ cm^{-2}.

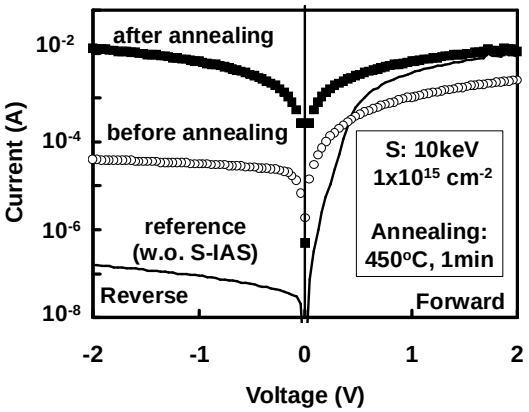

Fig.3: *IV* characteristics of NiPtSi/Si diodes before and after drive-in annealing. S-IAS process is not applied for the reference.

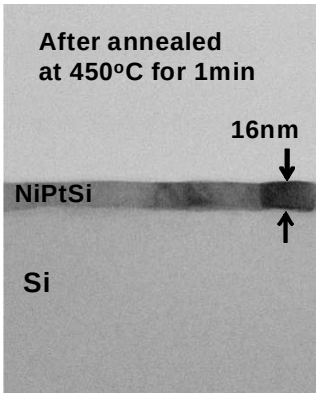

Fig.4: TEM image of NiPtSi/Si after drive-in annealing. S implantation dose is $1x10^{15}$ cm^{-2}.

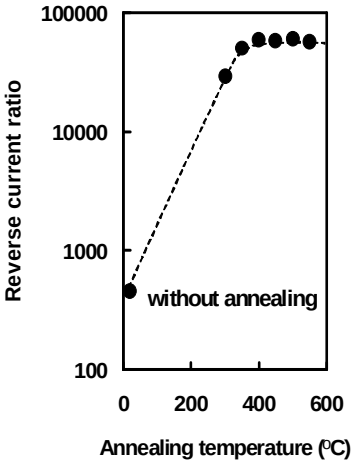

Fig.5: Annealing temperature dependence of reverse current ratio to the reference NiPtSi/Si at bias voltage of -0.5V.

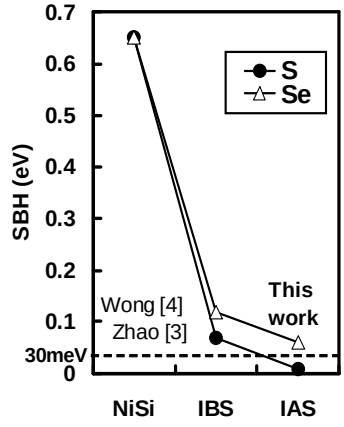

Fig.6: Comparison of SBHs obtained by IAS process and those of previous works.

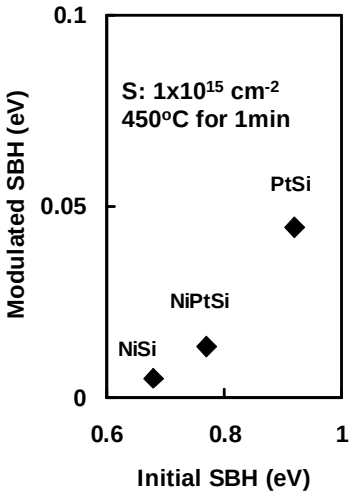

Fig.7: SBHs modulated by S-IAS process as a function of initial SBHs (without S-IAS).

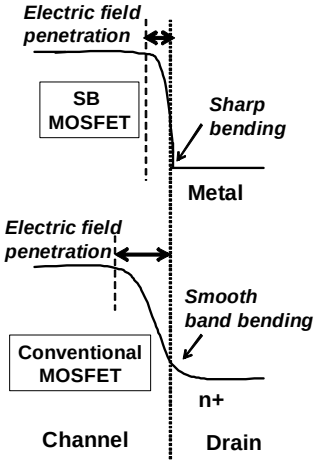

Fig.10: Schematics of the band bending at the drain edge of SB and conventional MOSFETs.

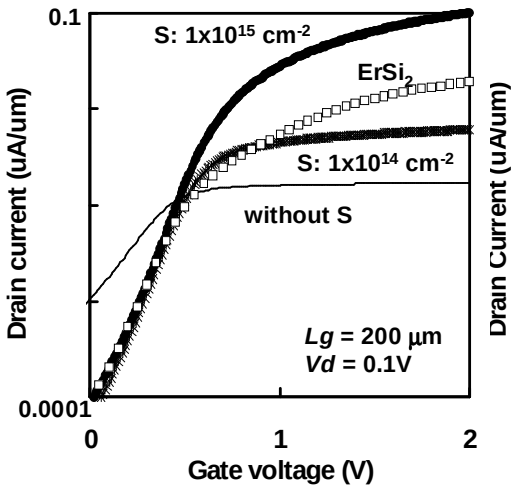

Fig.8: I_d-V_g characteristics of NiSi SB n-MOSFETs with and without S-IAS process, and $ErSi_2$ SB n-MOSFETs.

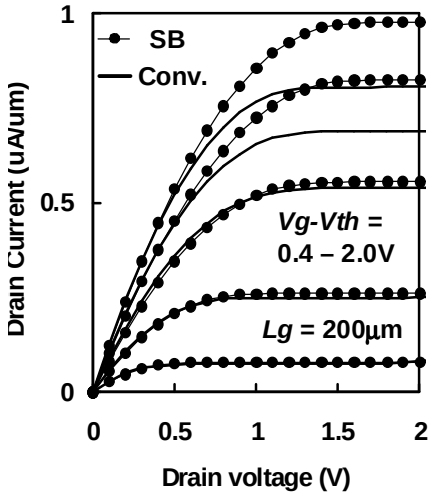

Fig.9:Comparison of I_d-V_d characteristics of S-IAS NiSi SB (dots with line) and conventional (solid line) MOSFETs.

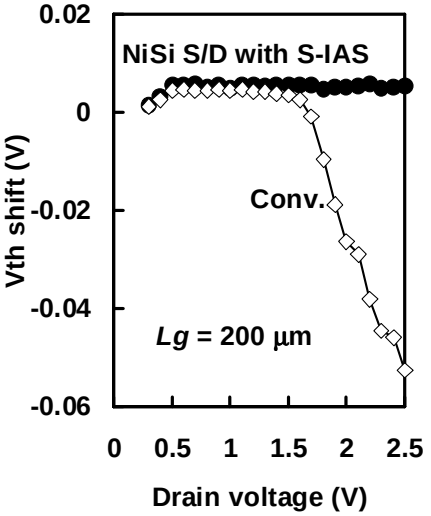

Fig.11: V_{th} shift as a function of drain voltage for S-IAS NiSi SB and conventional MOSFETs..