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A New Diamond-like Carbon (DLC) Ultra-High Stress Liner Technology for Direct Deposition on P-Channel Field-Effect Transistors

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Abstract

We report the first demonstration of a Diamond-Like Carbon (DLC) compressive-stress liner *directly deposited* on p-channel Field-Effect Transistor (p-FET). All previous technology demonstrations of the DLC high-stress liner technology employed a SiO_2 layer with a thickness of ~10 nm between the DLC and the p-FET. The new DLC technology reported here eliminates the SiO_2 layer, provides better scalability, simpler process integration, and possibly higher stress coupling efficiency. Integration of the DLC liner in strained p-FETs led to a significant drive current enhancement of 39% over unstrained control p-FETs.

1. INTRODUCTION

Diamond-like carbon (DLC) has a much higher intrinsic compressive stress (5 to 6 GPa) than the conventional SiN (≤ 3.5 GPa). DLC has been demonstrated as a high-stress liner on p-channel MOSFETs with various device structures, including planar, SOI, and multi-gate devices [1]-[4]. DLC has also been combined with other stressors such as SiGe source and drain (S/D) stressors [5]. However, in the initial stage of development for the DLC liner technology, a SiO_2 liner was inserted between DLC liner and the underlying p-FET for possible improvement of adhesion. However, this compromises the scalability and process simplicity of DLC technology, and may also reduce the channel stress induced by the DLC liner, especially when the SiO_2 layer is too thick.

In this paper, we report the first demonstration of the direct deposition of DLC high stress liner on p-FETs for enhancement of hole mobility and drive current performance. Process development efforts will be discussed. We will investigate the performance enhancement brought by the improved DLC liner technology.

2. MATERIALS CHARACTERIZATION

DLC films were deposited on 8-inch bulk Si substrates using a filtered cathodic arc (FCA) deposition system. Various substrate biases were applied, and the DLC films were characterized using UV Raman Spectroscopy. A higher sp^3 content in DLC generally gives a more insulating film (lower conductivity) and higher intrinsic stress. DLC films with high sp^3 content show two peaks in their UV Raman spectrum, one at ~1100 cm^{-1} (referred to as "T" peak), the other at ~1600 cm^{-1} (referred to as "G" peak) (Fig. 1), having intensities I_T and I_G, respectively. A substrate bias of 95 V was selected for device integration as it gives a G peak position that is most shifted to the right (Fig. 1) as well as the highest value for $I_T/(I_T+I_G)$ (Fig. 2), both indicating high sp^3 content [6].

3. DEVICE FABRICATION

P-FETs used in this study were fabricated on eight-inch bulk Si substrates. Schematics of p-FETs studied here are shown in Fig. 3 (a)-(c). After forming the gate stack (pre-doped poly-Si on ~2.6 nm SiO_2) and S/D extension, SiN spacers were formed with a SiO_2 spacer liner. Nickel salicidation was then performed. For p-FETs in Fig. 3 (b) and (c), a DLC film with a thickness of ~33 nm or ~26 nm respectively, was directly deposited on p-FET devices under a substrate bias of 95 V. DLC having ~5 GPa intrinsic compressive stress was adopted in this work. Contact formation was then performed to complete the device fabrication. DLC deposition conditions were optimized in consideration of intrinsic stress, resistivity, and adhesion. Strict measures of wafer cleaning and transfer of wafers to vacuum chamber were adopted for better adhesion between DLC liner and the underneath p-FET, as surface cleanliness was found to have a large impact on adhesion. Fig. 4 shows a TEM image of a p-FET (L_G = ~85 nm) with a ~33 nm thick DLC liner directly deposited on top. Good adhesion between the DLC liner and the p-FET was observed.

4. RESULTS AND DISCUSSION

Fig. 5 compares the I_{off}-I_{on} characteristics of p-FETs without DLC liner and with DLC liners having various thicknesses. Direct deposition of DLC liner with a thickness of ~33 nm and ~26 nm gives rise to 39 % and 16 % I_{on} enhancement, respectively, as compared with an unstrained control p-FET. Similarly, the $|I_{SD}|$-V_{DS} characteristics in Fig. 6 shows that a 43 % drain current enhancement is observed for p-FETs with ~33 nm DLC liner over the control p-FETs. P-FETs with ~26 nm DLC show a 19 % saturation drain current improvement. Fig. 7 shows that at V_{DS} = -50 mV and V_{GS} = -1 V, the linear drain current enhancement is 70 % and 36 % for p-FETs with a DLC liner thickness of ~33 nm and ~26 nm, respectively. Fig. 8 compares the transconductance of strained and unstrained p-FETs. A peak transconductance enhancement of ~90 % was observed on p-FET with ~33 nm DLC liner, indicating substantial hole carrier mobility enhancement. Fig. 9 shows that at a fixed Drain Induced Barrier Lowering (DIBL) of 150 mV/V, the saturation drain current taken at a gate overdrive (V_{GS}-V_T) of -1 V is enhanced by 56 % and 25 % for p-FETs with DLC liner thickness of ~33 nm and ~26 nm, respectively. Fig. 10 demonstrates that there are no significant differences in DIBL among strained and unstrained p-FETs. Fig. 11 compares saturation threshold voltage of p-FETs with and without DLC liner, with $V_{T,sat}$ taken at $|I_{SD}|$ = 100 nA×W/L_G, where W is the gate width. It can be observed that a thicker DLC liner, presumably giving a higher channel stress, generally gives a smaller $V_{T,sat}$. Similarly, Fig. 12 shows that a higher channel stress results in smaller $V_{T,lin}$.

5. CONCLUSION

The first demonstration of a DLC compressive-stress liner *directly deposited* on p-FETs was reported. The new DLC technology does not employ a SiO_2 layer, providing better liner stressor scalability and simpler process integration, as compared with prior work. A drive current enhancement of 39 % was reported for strained p-FETs integrated with DLC liner, over unstrained control p-FETs.

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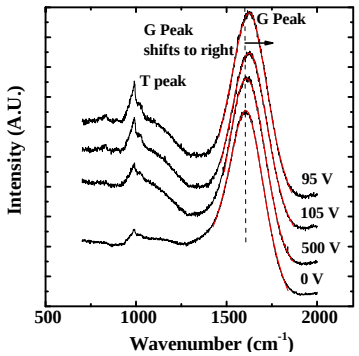

Fig. 1. UV (325 nm) excited Raman spectra of DLC films formed using different substrate biases. Referring to curves from bottom to top, the G peak position shifts right, indicating an increase in sp^3 content.

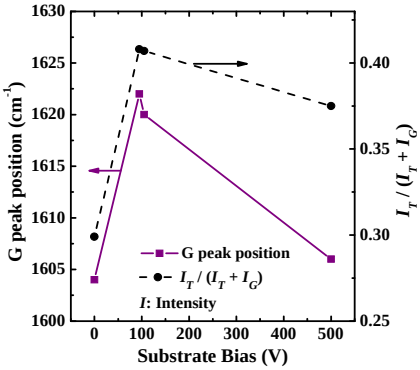

Fig. 2. G peak position and $I_T/(I_T+I_G)$ versus substrate bias. For the substrate bias of 95 V, the largest $I_T/(I_T+I_G)$ value was obtained, indicating high sp^3 content.

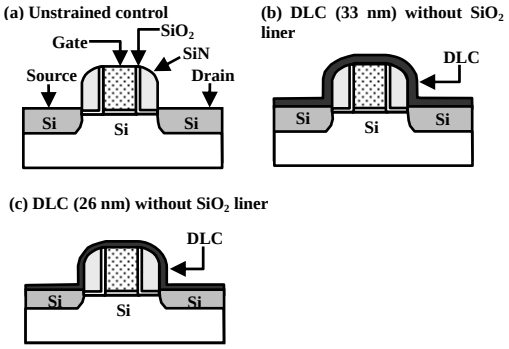

Fig. 3. Device cross-section for (a) unstrained control p-FET, (b) p-FET with ~33 nm DLC liner, and (c) p-FET with ~26 nm DLC liner.

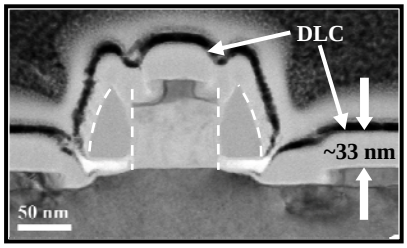

Fig. 4. TEM image of p-FET with ~33 nm DLC liner. DLC liner is directly deposited on p-FET without a SiO_2 liner. Good adhesion is observed.

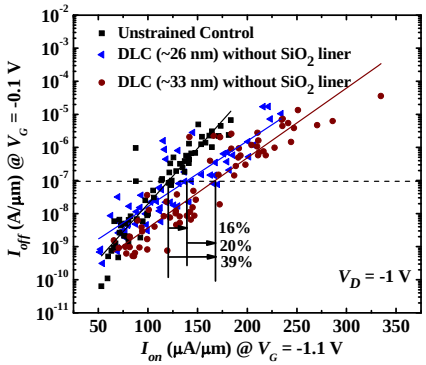

Fig. 5. I_{off} versus I_{on} for p-FETs with different DLC liner thicknesses and control p-FET. P-FETs with DLC liner of ~33 nm and ~26 nm have 39 % and 16 % higher I_{on}, respectively, than the control.

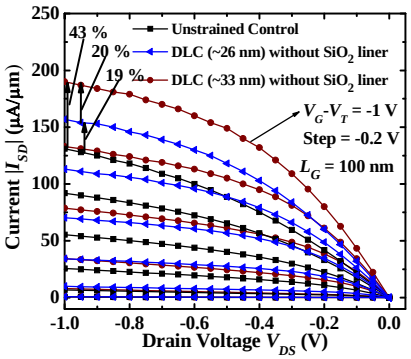

Fig. 6. P-FETs with ~33 nm DLC liner and ~26 nm DLC liner show 43 % and 19 % higher I_{on}, respectively, than a control at a gate overdrive of -1 V. I_{off} is 100 mA/μm for all devices.

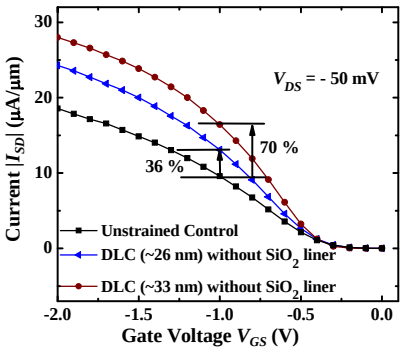

Fig. 7. $|I_{SD}|$ versus V_{GS} for different p-FETs at V_{DS} = -50 mV. P-FETs with DLC liner of ~33 nm and ~26 nm have 70 % and 36 % higher I_{SD} than control p-FET, respectively.

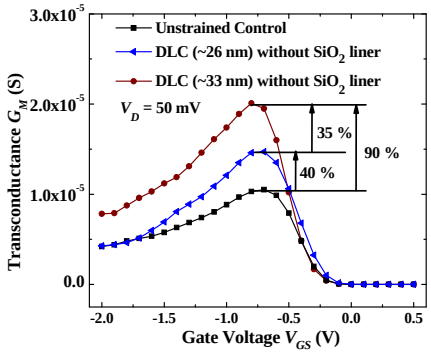

Fig. 8. Peak transconductance increases by 40 % and 90 % for p-FETs with ~26 nm and ~33 nm DLC liners, respectively, as compared with control.

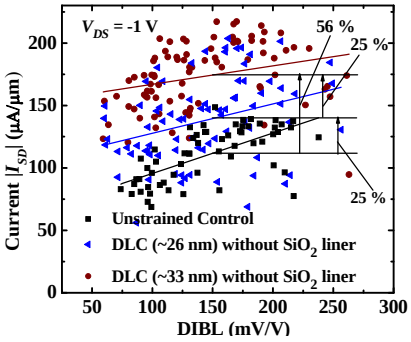

Fig. 9. At a fixed DIBL of 150 mV/V and V_{DS} of -1 V, DLC liner provides up to 56 % I_{SD} (taken at V_{GS}-V_T = -1 V) enhancement.

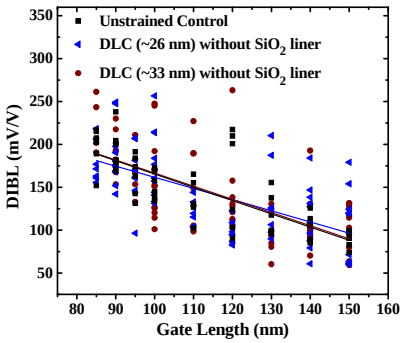

Fig. 10. DIBL versus gate length for p-FETs with and without DLC liner.

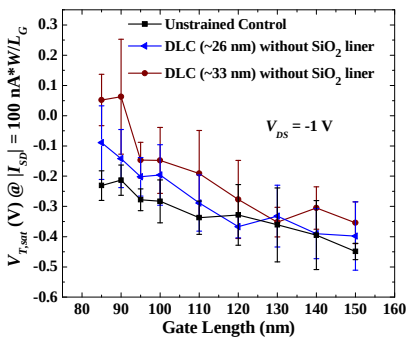

Fig. 11. $V_{t,sat}$ versus gate length, showing that higher strain leads to smaller $V_{t,sat}$. The error bar is the standard derivation.

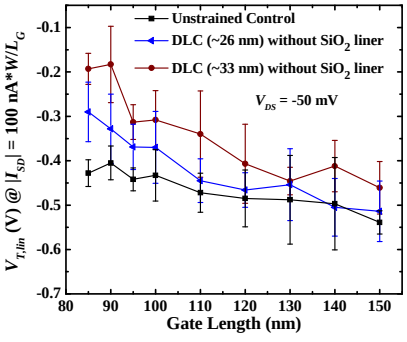

Fig. 12. $V_{t,lin}$ versus gate length, showing that higher strain leads to smaller $V_{t,lin}$. The error bar is the standard derivation.