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Investigation on Enhanced Impact Ionization in Uniaxially Strained Si MOSFET

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1. Introduction

Strained Si provides promising technology to promote performance enhancement of short channel MOSFET. Recently, besides digital application, strained Si technology attracting a great deal of attention in analog CMOS application such as RF power amplifier in the millimeter wave range. In the application of stained Si technology to power amplifier, impact ionization (II) is an important consideration because it determines breakdown voltage and, therefore, power gain. Recently, several groups have reported strain dependent impact ionization [1-4]. In fact reduction of breakdown voltage of SOI MOSFET with application of uniaxial strain has been reported [1]. As was extensively studied for biaxially strained Si on SiGe virtual substrate, the impact ionization threshold β, which is determined by the bandgap and the mean free pass of carriers, is reduced with tensile strain [2]. The reduction of β should enhance the impact ionization. However, the impact ionization is also a function of the maximum electric field E_m near the drain junction. Therefore, it is important for design of strained-Si MOSFET amplifier to clarify what the most critical parameter for estimating breakdown voltage is.

In this paper, we investigate change in impact ionization efficiency (IIE) with uniaxial strain and temperature using SOI and bulk MOSFET. We analyze experimental results from the view points of the ionization threshold β and maximum electric field E_m to clarify the parameter of major concern.

2. Experiment

MOEFETs were fabricated on SOI and bulk Si wafers using a standard process. SOI MOSFETs were of partially depleted type. Substrate current of SOI MOSFET was measured by forming the body tie structure. To reduce the resistance between the body and body contacts, body ties were formed at the both sides of the channel, as shown in Fig. 1(c). The channel length was 10 μm, which is long enough to avoid the effects of saturation velocity of carriers in the channel and parasitic source/drain resistance. The channel width was either 2 μm or 3 μm.

Uniaxial tensile strain up to about 0.2% was induced by applying bending deformation to a test chip using a cantilever structure. The experimental setup to apply the bending deformation using a cantilever is schematically shown in Fig. 1(a) and is equipped with a heater which enables us to elevate the temperature of the sample during application of strain. Strain was applied either in a direction longitudinal or transverse to the MOSFET channel which was aligned with <110> direction on the (100) surface.

Ionization threshold β and drain saturation voltage V_{DSAT} were extracted from substrate current model of MOSFET [5].

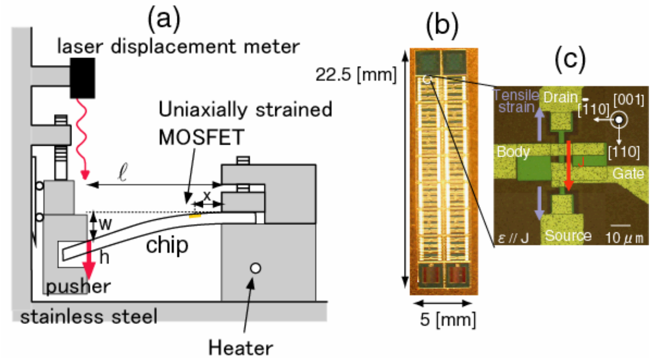

Fig. 1: (a) Schematic of cantilever bending tool constructed for the experiment which enables us to change temperature of the sample during application of strain. (b) Photo of an SOI chip containing MOSFETs. (c) Photomicrograph of a MOSFET in which twin-body was formed to reduce the body-tie resistance.

3. Results and discussion

It has been confirmed that, as shown Fig. 2, transconductance g_m increases and accordingly breakdown voltage decreases when uniaxial tensile strain is applied to the SOI MOSFET.

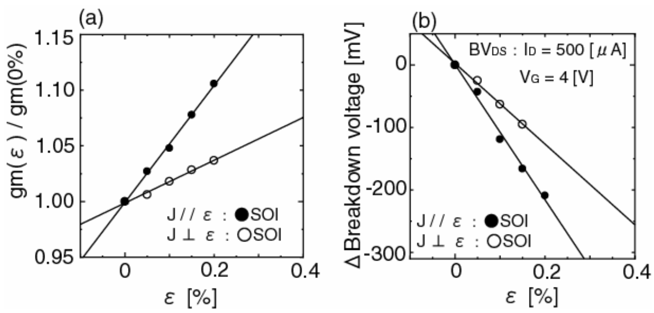

Fig. 2: Change with uniaxial tensile strain in transconductance g_m (a) and breakdown voltage (b) of an SOI MOSFET.

Figure 3(a) shows strain dependence of ionization threshold β. β was found to slightly decrease with tensile strain and no significant difference in decrease is observed between longitudinal strain and transverse strain. On the other hand, as shown in Fig. 3(b), drain saturation voltage V_{DSAT} decreases with tensile strain and the decrease is more pronounced in the case under the application of longitudinal strain than in the case under the application of transverse strain.

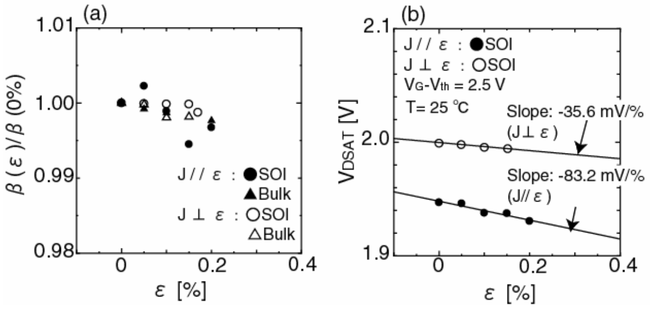

Fig. 3: (a) Uniaxial tensile strain dependence on β. (b) Uniaxial tensile strain dependence on V_{DSAT}.

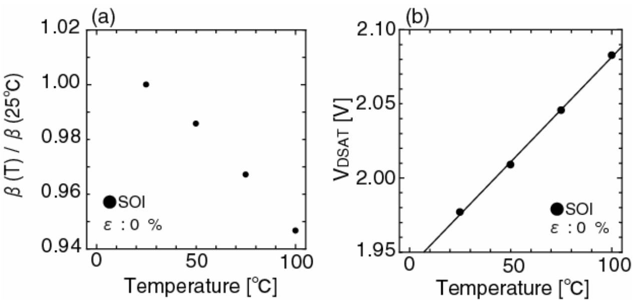

Fig. 4: (a) Temperature dependence on β. (b) Temperature dependence on V_{DSAT}.

Figure 4 shows temperature dependence of β and V_{DSAT}. β clearly decreases with elevating temperature. According to the substrate current model, when β decreases, impact ionization rate increases. On the other hand, V_{DSAT} was found to increase with increase of temperature. When V_{DSAT} increases, the maximum electric field E_m decreases because the potential difference in the drain depletion region, V_D-V_{DSAT}, decreases. Results shown in Fig. 4 suggest that if the change of β is of major concern impact ionization increases with elevating temperature, and vice-versa for V_{DSAT} .

We evaluated multiplication factor, M-1$(=I_{sub}/I_D)$, to find out which parameter, β or E_m, is significant for impact ionization. This factor shows integral of ionization rate in the high electric field, and increase of this factor means that impact ionization increases.

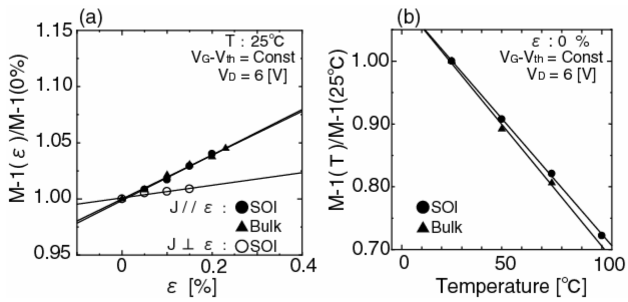

Fig. 5: (a) Dependence on uniaxial tensile strain of M-1.(b) Temperature dependence of M-1. M-1 values were measured under constant V_G-V_{th} and V_D.

Figure 5 shows uniaxial tensile strain and temperature dependence of M-1. In Fig. 5(a), we can clearly find that M-1 increases when tensile strain increase, and the increase was lager under longitudinal strain than under transverse strain. This indicates that impact ionization is different between longitudinal strain and transverse strain.

In Fig. 5(b), we find that M-1 decreases when temperature increases. This indicates that impact ionization decreases with elevating temperature. These results of strain and temperature dependence of M-1 are consistent with the change in V_{DSAT}. Therefore, we can say that the enhanced impact ionization in strained Si MOSFET is mostly induced not by change in ionization threshold β but by change in E_m due to change in V_{DSAT}.

To complete our discussion, we should clarify the reason why V_{DSAT} changes with strain and temperature. Figure 6 shows change in maximum field near the drain with increasing carrier mobility and temperature. We can see that the maximum field increases with increasing mobility and decreasing temperature. These results indicate that the potential drop along the channel and, therefore, V_{DSAT} decreases due to strain induced increase in carrier mobility.

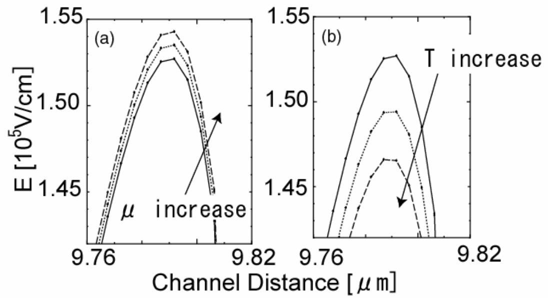

Fig. 6: Simulation results of variation of maximum electric field along the channel with carrier mobility (a) and device temperature (b). The results are consistent with experimentally observed variation in V_{DSAT}.

4. Conclusion

We investigated change in impact ionization rate with uniaxial strain in terms of ionization threshold β and maximum electric field E_m. We found that, while β is surely decreases with the application of strain, the change in β is of minor concern and the change in E_m which increases due to strain induced increase in carrier mobility practically determines the impact ionization rate. This knowledge will be useful in particular for design of MOSFET for power amplifier application.

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