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Influence of Carrier Transit Delay on CMOS Switching Performance

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1. Introduction

It has been reported that the loss in gate overdrive prevents switching-speed improvement in advanced technologies [1, 2]. For such cases it has been reported that the ring-oscillator delay cannot be predicted by the conventional I_{half} method, from the DC MOSFET current at V_{gs}=V_{DD} and V_{ds}=V_{DD}/2. Instead I_{peak}, estimated by circuit simulation at V_{out}=V_{DD}/2 of the ring-oscillator stage, was found to be more appropriate to capture the gate-overdrive loss as schematically shown in Fig. 1 [1]. Here we investigate the origin of I_{peak} in the inverter, the basic element of the ring-oscillator. It will be shown that the switching delay is in fact physically determined by the MOSFET's displacement current at higher frequencies, which reduces the influence of the DC current on the switching delay.

2. Estimation of Inverter Delay

Fig. 2 shows measured current responses of a nMOSFET and a pMOSFET with a gate length of 10μm. Simulated results with HiSIM are depicted together. HiSIM is a compact MOSFET model based on the surface-potential description in a similar way as 2D-device simulators. For the simulation HiSIM model parameters are extracted with measured *I-V* characteristics. The error of the extracted model parameter sets is kept within 1%. The accuracy of switching performance for both nMOS and pMOS has been verified with measurements as seen in Fig. 2.

Conventionally, the inverter delay is estimated by the I_{half} method with the simple equation

$$T_{pd,half} = \frac{C_L V_{DD}}{I_{half}} \tag{1}$$

However, this equation was found to be invalid for advanced technologies with small V_{th}, and an alternative description has been proposed as

$$T_{pd,peak} = \frac{C_L V_{DD}}{I_{peak}} \tag{2}$$

where I_{peak} is the current flowing during the switching process at V_{out}=V_{DD}/2. Here the problem is that I_{peak} can be known only through circuit simulation and its origin cannot be determined easily.

Fig. 3 shows a simulated switching waveform of the inverter for very slow switching speed, verifying that I_{peak} currents during switch-high and switch-low are approximately equal. The suppressed magnitude of I_{peak} reveals that a lot of energy is lost during switching by large currents which directly flow from high supply voltage (V_{DD}) to low supply voltage (GND) as depicted in Fig. 4 by vertical arrows. The load capacitance C_L is selected to be about the same as sum of the gate-oxide capacitances of nMOS and pMOS (fan-out 1), namely 911fF for the studied case of MOS dimensions.

Fig. 5 compares the inverter delay, estimated with different methods, as a function of the switching speed. For the comparison simulated delay $T_{pd,sim}$ with a circuit simulator is also depicted. While the I_{half}-method wrongly predicts a switching-speed independent delay, the I_{peak}-method is close to the accurate compact-model result for higher switching speed, but somewhat off for very low switching-speed.

3. Delay Mechanism in Inverter

Fig. 6 summarizes current flows during the switching, and verifies that I_{peak} is much smaller than I_{half} as expected. Under very slow switching I_{peak} is approximately the current under the V_{gs}=V_{ds}=V_{DD}/2 condition. However, I_{peak} increases as the switching speed increases and the current flows only between load capacitance and nMOS during switch-high and between the pMOS and load capacitance during switch-low. The magnitude of this current is increasingly determined by the displacement current, the second term on the right hand side equation for the transient current

$$I(t) = I_0(V(t)) + \frac{dQ}{dt} \tag{3}$$

where

$$\frac{dQ}{dt} = \frac{dq}{dV_{out}} \frac{dV_{out}}{dt} \tag{4}$$

and I_0 is the DC current and Q is the induced charge. Under the high-speed switching condition, the displacement current dominates over the conductive current, and governs the switching performance, and dq/dV_{out} becomes equal to C_L. Consequently, we can approximately predict the I_{peak} value analytically by approximating I_{peak}=I_{cap} =C_L dV_{out}/dt. The dV_{out}/dt can be analytically written

$$I_{peak} = I_{ds}(V_d = \frac{1}{2}V_{DD}, V_g = \frac{1}{2}V_{DD} + \frac{V_{DD} \times tau}{T_r}) \tag{5}$$

where tau is the transit delay determined by *L/v*.

4. Conclusions

We have investigated the I_{peak} current to predict the propagation delay of the inverter. It was found that the delay is governed not only by the transit current but also by the displacement current. An analytical description for predicting the I_{peak} current has been proposed.

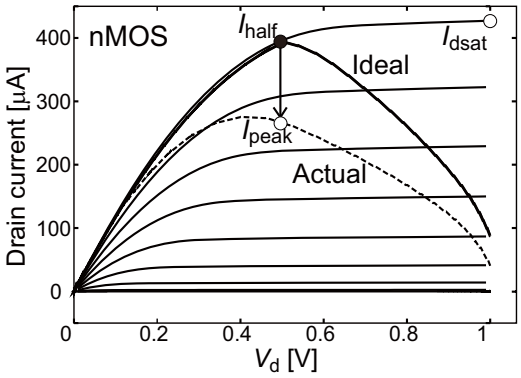

Fig. 1. Trajectories during inverter switching. "Ideal" means the conventionally known case described by the I_{half} method, and "Actual" means the case observed for advanced CMOS technologies.

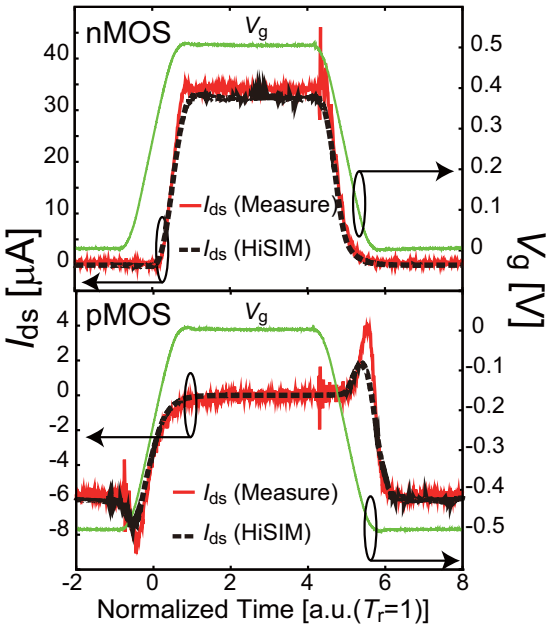

Fig. 2. Comparison of measured nMOS and pMOS switching performance with calculated HiSIM results.

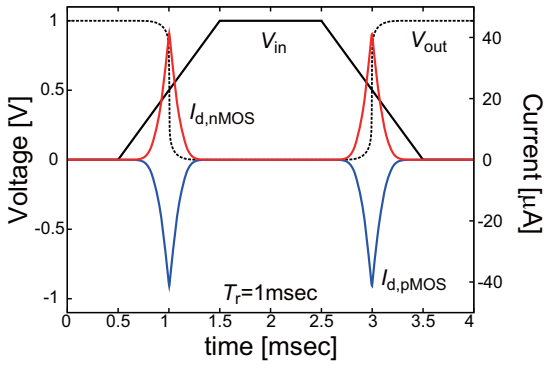

Fig. 3. Waveforms of the inverter switching with an extremely slow rise time T_r of 1msec. The fat solid line is the current flow in the nMOS and the fat dashed line is that in the pMOS. The peak currents are equal and referred to as I_{peak}.

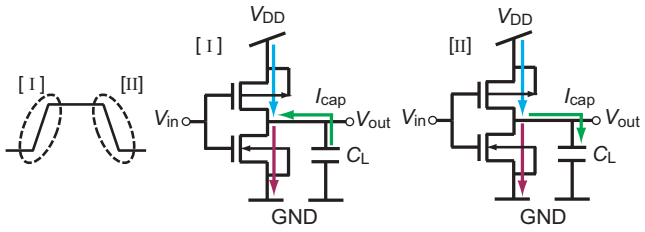

Fig. 4. Schematic diagram of the investigated inverter switching. The low of currents during switch-high [I] and during switch-low [II] is schematically shown.

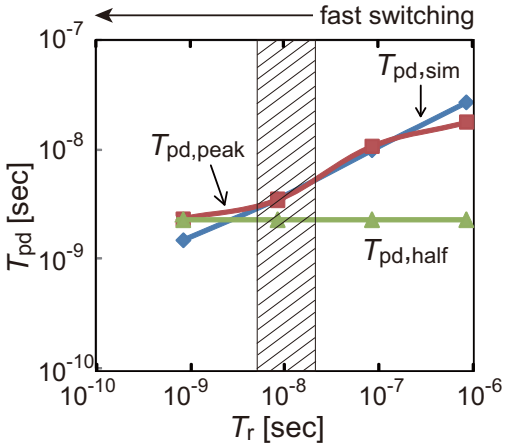

Fig. 5. Comparison of the propagation delay T_{pd} of the studied inverter calculated with different methods as a function of the switching-high speed T_r. $T_{pd,sim}$, $T_{pd,peak}$, and $T_{pd,half}$ are values determined with the compact model HiSIM and a circuit simulator, using Eq. (2), and Eq. (1), respectively. The shaded region holds simulated half periods normalized by the number of stages of ring oscillators in the horizontal axis for different stages of ring oscillators which consist of the studied inverters.

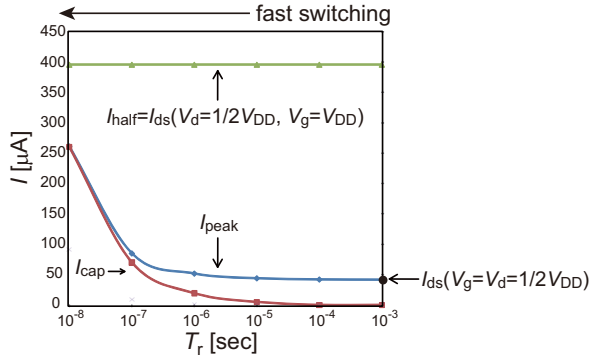

Fig. 6. Calculated currents determining the propagation delay of the inverter. I_{cap} is the current flowing from/to the load capacitance.

References

[1] E. Morifuji et al., Tech Digest IEDM, p.1049, 2005
[2] M. H. Na et al., Tech Digest IEDM, p.121, 2002