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Thermally stable Ni-silicide gate electrode with TiN barrier metal for NAND flash memory application with 24 nm technology and beyond

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1. Abstract

Ni-silicide with TiN barrier metal has been demonstrated for NAND flash memory devices with 24 nm technology node as a gate word line. When a TiN layer with 200 Å thickness by physical vapor deposition (PVD) is inserted in the control gate polysilicon, inter-diffusion of Ni and grain growth of NiSi are successfully suppressed. As results, no significant sheet resistance increase is observed even at the narrow gate line with 24nm width and its thermal stability is maintained up to 900 ℃.

2. Introduction

As the scalability is drastically down to 20 nm, the gate word line resistance is getting more important for RC delay. At 20 nm feature size, Ni-silicide is the most promising material as a gate word line because of less line width effect [1], low resistivity and lower Si consumption. However, NiSi can be only considered to be used at low thermal budget since it has high diffusion rate and poor thermal stability, meaning that the phase can be still modulated and affected by the following high thermal process. There have been many studies on improving thermal stability [2, 3] of NiSi by the additive elements, which act as retarding phase change into $NiSi_2$ (higher resistivity) or suppression of grain growth. But the improvement of thermal stability is not significantly effective because the excess Si exists under NiSi. Here, we have suggested the refractory metal compound (TiN) as a barrier metal layer in the control gate to achieve extremely high thermal stability up to 900 ℃.

3. Experiment

In this experiment, the control gate consisted of 3 layers (upper poly Si/TiN/bottom poly Si). A PVD TiN layer was used as a barrier metal. And cells of 24 nm were defined by spacer patterning technology (SPT). PVD Ni (Pt: 5 %) was deposited and followed by 2-step anneal to form NiSi.

4. Results

The cell width of 24 nm is estimated at the bottom of the floating gate so that the actual width of the control gate is a bit smaller than 24 nm. Fig. 1 shows the schematic drawings of the conventional NiSi and TiN barrier metal inserted structure. In case of conventional structure, the NiSi formation is not uniformly formed along the word line. Especially after thermal budget, the partial grain growth of NiSi down to the surface of inter poly dielectric (IPD) and the discontinuity of the NiSi along the word line occur, resulting in degradation of device performance and increase of Rs respectively.

Figure 2 shows the TEM images for both y- and x- cut view of the word line after NiSi formation on the conventional 24 nm patterned structure with various 1st anneal temperatures but same 2nd anneal temperature. It is observed that unnecessary Ni-fully silicidation (FUSI) formation occurred at 400 ℃ while partial NiSi is formed at lower temperature, implying that at the 24 nm feature size, the phase and thickness of NiSi were not effectively controlled. The sheet resistance is also extracted from the same structure and Rs decreases with increasing the 1st anneal temperature as shown in Fig 3. The evaluation of the thermal stability is performed with both Rs measurement (Fig. 3) and TEM (Fig. 4) analysis after the additional thermal budget by RTP. As the thermal budget is increased by 800 ℃, the NiSi grain contacts with the surface of the IPD layer, which may cause the severe degradation of IPD quality. In addition, the phase change and the discontinuity of NiSi are observed and the Rs increases dramatically at 900 ℃ (refer to Fig. 8). To overcome these problems, the concept of barrier metal layer insertion somewhere in the polysilicon is implemented. The role of the barrier metal layer is to confine the Si source and to suppress the inter-diffusion of Ni, resulting in no discontinuity of NiSi formation observed.

For a barrier metal, a TiN layer is chosen among several candidates, because it is thermodynamically and chemically stable. The roughness and chemical composition of TiN are detected by AFM (Fig. 5) and AES (Fig. 6) analysis respectively. It exhibits that the stoichiometric structure of the TiN layer is maintained even after 900 ℃ RTP anneal. Fig. 7 shows the TEM images of NiSi before and after 900 ℃ RTP anneal. Although the thermal budget is as high as 900 ℃, no NiSi is formed beneath the TiN and no Ni is detected by EDS (not shown here). Consequently, Rs increase is negligible up to 900 ℃ (Fig. 8), which means that the phase separation and discontinuity are successfully suppressed by the insertion of TiN layer as a barrier metal.

5. Conclusion

In this work, we confirm that the scalability of NiSi down to 24 nm and NiSi with TiN barrier metal is successfully defined and demonstrated for flash memory application. Results show that a stoichiometric TiN of 200 Å inserted in the control poly gate can suppress inter-diffusion of Ni and grain growth of NiSi, leading that significant thermal stability was achieved up to 900 ℃.

References

[1] J. A. Kittl, et al., VLSI Tech., 72 (2005) [2] T. Marukame, et al., IEDM, 547 (2008) [3] T. Sonehara, et al., IEDM, 921 (2008)

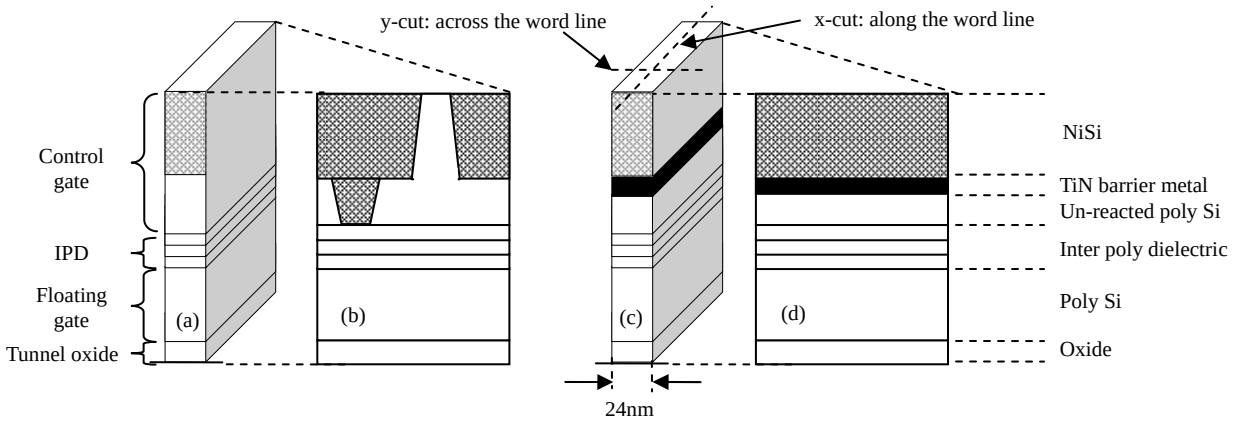

Fig 1. The schematic drawings of a conventional NiSi structure of 24nm: (a) y-cut view (across the word line), (b) x-cut view (along the word line)
The schematic drawings of a TiN barrier metal inserted NiSi structure of 24nm: (c) y-cut view, (d) x-cut view

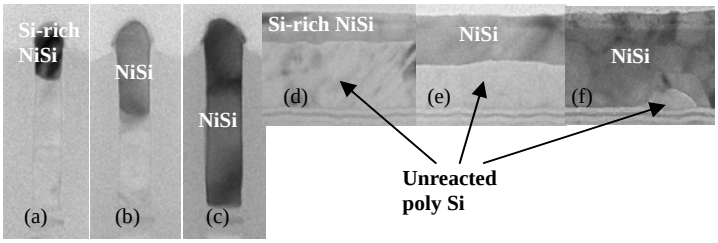

Fig. 2. TEM images illustrating the height of the NiSi formation at 24nm for various 1st anneal temperatures (y-cut view of the word line (a) at 300℃, (b) at 350℃, and (c) at 400℃). At 300℃, Si-rich silicide was formed and the NiSi thickness is too thin to acquire appropriate Rs but the interface between the NiSi and unreacted poly Si exhibits smooth (d). At 350℃, no FUSI was observed and the phase of the NiSi is uniform in depth with smooth interface (e) between the NiSi and unreacted poly Si. At 400℃, unnecessary Ni-FUSI was formed and only small area of the unreacted poly Si was observed (f).

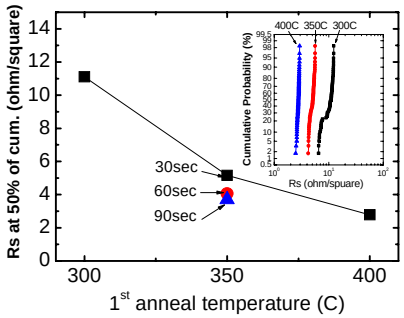

Fig. 3. 1st anneal temperature dependence of the sheet resistance for NiSi of 24nm without TiN barrier metal layer. For all samples, Rs was measured after NiSi formation using 2-step anneal process and 2nd anneal temperature was carried out at the same temperature. At 350℃, 1st anneal time dependence was also investigated. (inset: cumulative probability vs. Rs for various 1st anneal temperatures)

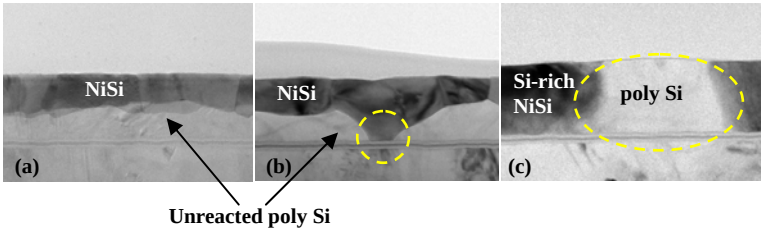

Fig 4. TEM images along the word line without barrier metal layer
(a) NiSi after 600℃ anneal by RTP shows relatively small grain size and no FUSI formation
(b) NiSi after 800℃ anneal by RTP shows bigger grains and partial FUSI formation
(c) NiSi after 900℃ anneal by RTP shows phase change and discontinuity of NiSi

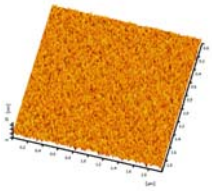

Fig 5. AFM analysis for PVD TiN
(RMS: 1.059nm)

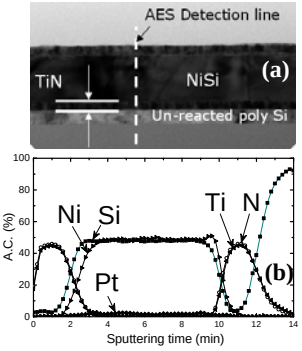

Fig 6. (a) TEM image after 900℃ anneal for a blanket sample (b) AES analysis for the NiSi after 900℃ anneal

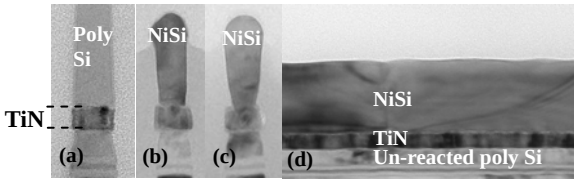

Fig. 7. TEM images of gate word line with TiN barrier metal
(a) Before Ni deposition (with 24nm cell patterned)
(b) As NiSi formation without following thermal budget
(c) NiSi after 900℃ RTP anneal. It shows no inter-diffusion of Ni (EDS data is not shown here) and no penetration of NiSi grains through the TiN barrier metal.
(d) Along the word line view of (c)

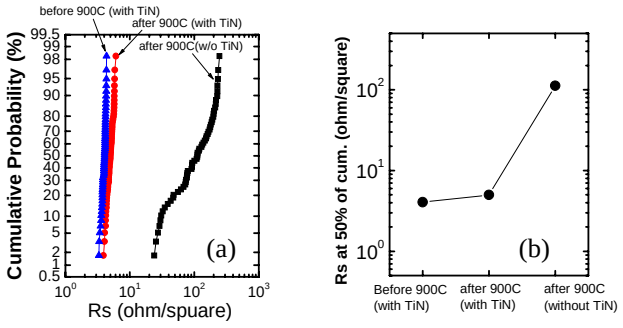

Fig. 8. (a) Cumulative probability vs. Rs of NiSi word line patterned with 24nm (b) Rs vs. various conditions for NiSi word line (before and after 900℃ thermal budget and with/without TiN barrier metal at 24nm