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Oxygen-Terminated Si Surface for Atomic Layer Deposition and its Impact on Interfacial Electrical Quality of sub-nm-EOT high-k Gate Stacks

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1. Introduction

The latest ULSI technology employs a multilayer gate stack structure consisting of high-k and thick interfacial SiO_2 layers. From the viewpoint of further scaling of equivalent oxide thickness (EOT), use of interlayer with higher dielectric constant than SiO_2 or high-k/Si 'direct-contact' gate stacks without a thick interlayer is expected to eliminate the increase in EOT [1-3]. In previous studies we reported that, in order to fabricate direct-contact high-k gate stacks, special attention needs to be paid to the surface chemical nature of Si prior to film growth by using atomic layer deposition (ALD), which has a marked impact on the electrical film quality of high-k [4,5].

We recently developed a surface etching technique that uses active oxidation, which is an etching reaction by O_2 with clean Si surfaces under high temperature and low O_2 pressure conditions (Fig. 1) [6-10]. Si etching by O_2 is known to be promoted by the adsorption of oxygen onto the Si dangling bonds, and the oxygen-terminated Si atoms desorb from the surface as SiO molecules [10]. In this paper we demonstrate the impact of this "oxygen-terminated Si surface" as the initial surface for high-k gate stacks from the viewpoint of interfacial electrical properties and surface bonding nature. The high-k gate stacks fabricated on the O-terminated surfaces showed excellent interfacial electrical quality, as directly evidenced by drastic suppression of hysteresis of capacitance-voltage (CV) characteristics on sub-nm-EOT HfO_2 gate stacks.

2. Experimental

Figure 1 shows a distribution map of active and passive oxidation of Si surface [7,8], and Fig. 2 shows an example of temperature dependence of Si(001) etching rate [6], which corresponds to condition (b) in Fig. 1. By lowering temperature, etching rate abruptly decreases to zero, which indicates that the reaction mode shifts from active to passive when passing through the boundary condition. Figure 3 shows variation in oxide thickness formed by active oxidation as measured by X-ray photoelectron spectroscopy, whose thicknesses were calculated with photoelectron escape depth of SiO_2. Around the boundary condition, an ultra-thin oxide-layer was maintained.

Figure 4(a) shows procedures of gate stack formation on an O-terminated surface, and (b) is a schematic structural model of the O-terminated surface. Generally, top chemical bonds of thick SiO_2 have not been discussed in detail but, in this model, O atoms terminate the tops of Si atoms. We also prepared (c) a hydrophilicized surface by H_2 desorption from HF-last surface followed by dissociative adsorption of H_2O to Si dangling bonds [4,5], and (e) an HF-last surface serving as a standard surface. Surface preparation and atomic structures of these surfaces are also shown in Fig. 4(c)-(f). On these three types of initial surfaces, we fabricated NiSi gate high-k capacitor/FET by means of a gate last process. HfO_2 gate dielectric layers were grown by means of ALD at 250˚C, with $Hf[N(CH_3)_2]_4$ and H_2O serving as precursors.

3. Results and discussion

Figure 5 shows results of (a) leakage current (Jg)-V and (b) CV measurements of HfO_2 gate stacks fabricated on surfaces prepared by O-termination, dissociative adsorption of H_2O, and HF-last, respectively. On the HF-last surface, abnormally large leakage current was observed [4,5], whose origin was explained as pinhole generation in the ALD-high-k layer grown on a hydrophobic surface. By changing the chemical nature of the surface, the large leakage current was drastically suppressed. In (b), the very poor electrical properties due to leakage current on the HF-last surface was improved on hydrophilicized surfaces. Moreover, that on the O-terminated surface showed better electrical properties. Figure 6 shows variation of CV hysteresis at flatband voltage (V_{FB}). On the surface hydrophilicized by dissociative adsorption of H_2O, leakage current can be reduced as compared with the HF-last surface (Fig. 5(a)), but the magnitude of CV hysteresis was still large. On the other hand, the CV hysteresis shows a drastic decrease on the O-terminated surface in comparison with other surfaces. These features directly reflect the decrease of traps at the interface and high-k film. Figure 7 shows variations of EOT for the HfO_2 gate stacks. By using the O-terminated surface, improvement of electrical properties can be realized without significant increase of EOT, whose value can be scaled to 0.61 nm with small CV hysteresis. Figure 8 shows EOT-Jg characteristics of HfO_2 gate stacks, which also shows no Jg degradation on O-terminated surface. Figure 9 shows electron mobility comparison of HfO_2 FETs. The electron mobility at 0.8 MV/cm on the O-terminated surface shows ~47% improvement against that observed for H_2O adsorption.

Table-I shows a score sheet of electrical properties on three initial surfaces. On the hydrophobic surface, unfavorable ALD growth, such as island-like growth, initiates pinhole generation or traps at the interface. The O-terminated surface shows the best performance for ALD-high-k gate stack formation. We suppose that a decrease of Si-H bonds on the surface would affect improved electrical properties, because dense HfO_2 formation at the interface would realize a decrease of traps at the interface.

4. Summary

We presented the impact of a novel oxygen-terminated Si surface prior to ALD-high-k growth on the interfacial electrical quality of sub-nm-EOT high-k gate stacks. The EOT value of the $NiSi/HfO_2/Si$ gate stack on the O-terminated surface can be scaled to 0.61 nm with small CV hysteresis.

Acknowledgements

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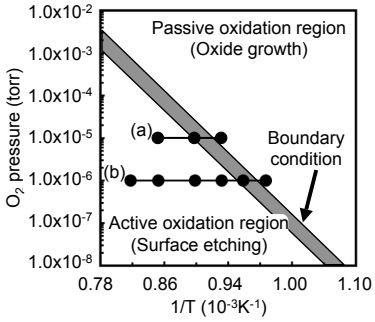

Fig. 1 Schematic distribution map of active and passive oxidation [7,8]. Active oxidation is an etching reaction by O_2 with clean Si surfaces, and formation of SiO_2 is generally called passive oxidation. The grey area corresponds to the boundary condition region between active and passive regions.

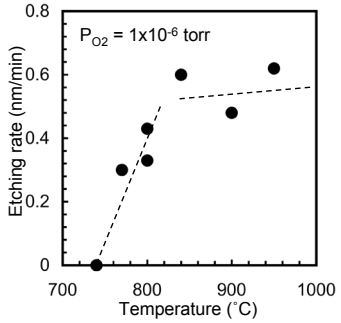

Fig. 2 Temperature dependence of O_2 etching rate. O_2 pressure was $1x10^{-6}$ torr. Experimental conditions correspond to (b) in Fig. 1.

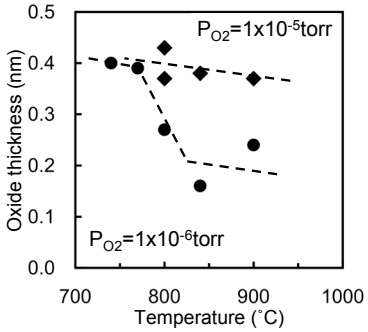

Fig. 3 Oxide thickness due to active oxidation, as measured by XPS. Photoelectron escape depth of SiO_2 was used for the analysis. Experimental conditions correspond to (a) and (b) in Fig. 1.

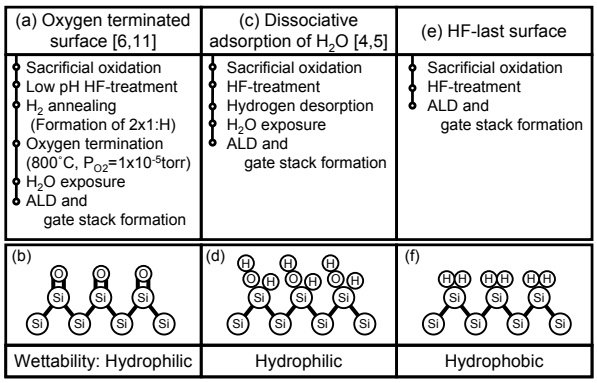

Fig. 4 Experimental procedures and structural models of surfaces prepared by O-termination, dissociative adsorption of H_2O, and HF-last, respectively. The chemical nature of each surface is also described. After these treatments, NiSi gate high-k gate stacks were fabricated by means of the gate first process.

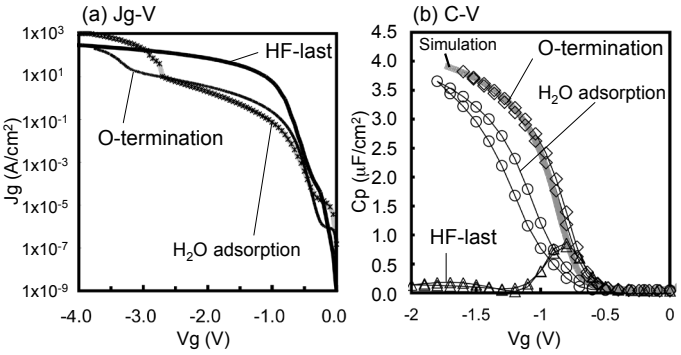

Fig. 5 (a) Jg-V and (b) C-V measurements of HfO_2 gate stacks on three types of initial surfaces. Thickness of HfO_2 is 2.4nm. Post deposition annealing was performed after ALD at 750˚C in purified N_2 flow. In (b), a simulated CV curve is indicated by the grey line. CV curve of the O-terminated surface shows good agreement with the simulated curve.

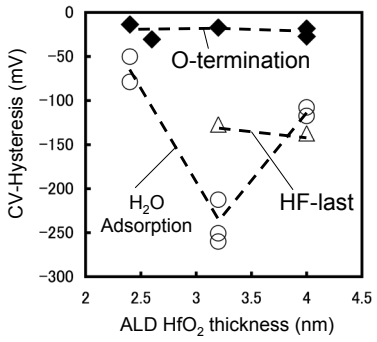

Fig. 6 CV hysteresis at V_{FB} of HfO_2 gate stack depending on HfO_2 thickness on three types of initial surfaces. A negative hysteresis value corresponds to counterclockwise sweep feature of CV (Fig. 5(b)).

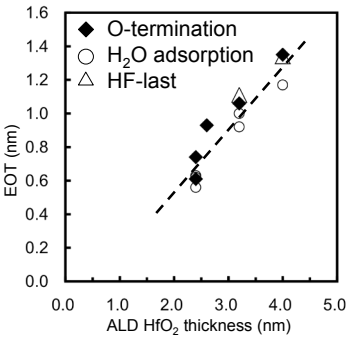

Fig. 7 EOT of HfO_2 gate stacks on three types of initial surfaces depending on HfO_2 thickness.

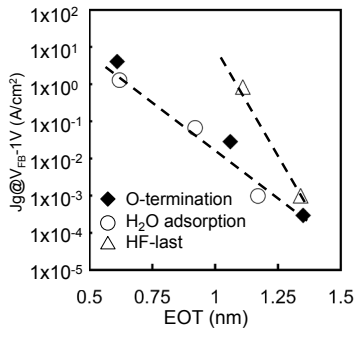

Fig. 8 EOT-Jg plot of HfO_2 gate stacks on three types of initial surfaces.

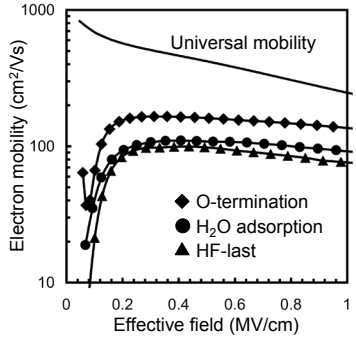

Fig. 9 Comparison of electron mobility of HfO_2 FETs on three types of initial surfaces. Thickness of HfO_2 is 3.2 nm.

Surfaces	O-termination	H_2O adsorption	HF-last
Chemical bonding of top surfaces	SiO	SiH, SiOH	SiH
Wettability	Hydrophilic	Hydrophilic	Hydrophobic
Jg of high-k gate stacks	○ Suppressed	○ Suppressed	X Large
CV-hysteresis of high-k gate stacks	○ Suppressed	X Large	X Large

Table-I Score sheet for electrical properties of HfO_2/Si gate stacks fabricated on three types of initial surfaces.