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New Criteria for Suppressing Extrinsic Defect Generation in Ultra Thin SiON Gate Insulator (EOT<1.4nm) for Advanced CMOSFETs

Satoshi Shimamoto[1], Hiroshi Kawashima[2], Toshiyuki Kikuchi[1], Yasuo Yamaguchi[2] and Atsushi Hiraiwa[2]

[1]Micro Device Division, Hitachi, Ltd., 6-16-3, Shinmachi Ome-shi, Tokyo 198-8512, Japan
Phone: +81-428-33-2222(ext.5174) E-mail:satoshi.shimamoto.xh@hitachi.com
[2]Renesas Technology Corp., 751 Horiguchi, Hitachinaka, Ibaraki 312-8504, Japan

1. Introduction

Reliability of MOSFETs is attracting more and more attention of LSI engineers in accordance with the decrease in the gate insulator thickness. The gate insulator breakdown is one of the key reliability issues. Most of the previous studies focused on the intrinsic breakdown caused by voltage stresses, the so-called time dependence dielectric breakdown (TDDB)[1].

On the other hand, little attention has previously been paid to the extrinsic defects that are inevitably built in the gate insulators during the fabrication process. The situation might have been brought about by the empirical fact that the number of extrinsic defects decreases when the gate insulator becomes thinner. Additionally, the leakage current caused by the extrinsic defects, if any, is masked by the gate leakage current that flows through the intrinsic portion of the test structures. These facts have distracted reliability-engineers' attention from the extrinsic defects.

In this study, we investigated the extrinsic defects built in SiON gate insulators with EOT<1.4nm by measuring the minimum supply voltage (V_{ddmin}) for normal operation of logic test RAMs. We propose the critical parameter to maintain low defect density, which is very important in mass production of the CMOS devices using ultra thin SiON gate insulator for 65nm-node technology and beyond. Furthermore, we analyzed the defects generation mechanism by applying the Percolation theory [2].

2. Experimental

We fabricated the 256Kbit test RAMs that consist of elemental unit of CMOS logic circuits and measured the V_{ddmin} for normal operation of all the bits. These test RAMs were designed so that the variation of MOSFET's resistance between gate and substrate due to gate leakage can be sensitively detected as the increase of V_{ddmin}. By censoring V_{ddmin}, gate leakage of even one MOSFET in 256Kbit RAMs can be detected.

The SiON gate insulators were formed by successively applying base oxidation (BO), plasma nitridation (PN) and post nitridation anneal (PNA) [3,4]. The thickness was ellipsometrically measured by assuming that the refractive index is equal to that of SiO_2, namely 1.465. The thickness thus measured is not equal to the physical thickness or to the equivalent oxide thickness (EOT), and is called "optical thickness (d_{opt})" in this study. We formed SiON gate insulator with various d_{opt} and EOT by changing the BO, PN, and PNA conditions for the typical 65nm-node LOP CMOSFETs (L_g=50 nm, V_{dd}=1.0V). EOT was determined by the CV fitting method [5].

3. Results and Discussions

Fig.1 shows an example of cumulative distributions of V_{ddmin} of test RAMs. Each set of data represents the result on about 130 dies fabricated on the same wafer. We can clearly observe tail components in a large-V_{ddmin} region separately from main distributions. We analyzed the large-V_{ddmin} dies by using a nanoprober and SEM. An example of nanoprober measurements is shown in Fig.2. MOSFET gate leakage current of the fail bit in large-V_{ddmin} die shows abnormal increase to ~μA range. The small gate leakage of ~μA undetectable in the conventional method is successfully detected. Fig.3 shows a plan view of a large-V_{ddmin} bit as observed by using an SEM after selectively etching off the Poly-Si gate electrodes. We notice an irregular dark pattern that is formed in the Si substrate by the attack of gate electrode-etchant through a pinhole in the gate insulator. From these results, we confirmed that the increase of V_{ddmin} is caused by the extrinsic defects.

Fig.4 shows the fraction of V_{ddmin}-failure on each wafer as a function of process time of PN and PNA. V_{ddmin}-failure depends on the process conditions sensitively. Fig.5 shows the fraction of V_{ddmin}-failure as a function of gate leakage current of NMOSFET (J_{gn}), EOT and d_{opt}. As seen from the Fig.5, it correlates weakly with J_{gn} or EOT but strongly with d_{opt}. If d_{opt} becomes thinner than ~1.7nm, defect density increases rapidly. As a result, we found that it is very important to keep d_{opt} as thick as possible without degrading other performance parameters (J_g, I_{ds} and NBTI) from a reliability standpoint. In order to optimize the process conditions under this guideline, we analyzed the variations of d_{opt} and EOT (Δd_{opt} and ΔEOT) by changing BO, PN and PNA process conditions. The relationships between Δd_{opt} and ΔEOT are shown in Fig.6. In order to increase d_{opt} without degrading I_{ds}, ΔEOT should be kept to a minimum. From this standpoint, increase of PN time seems to be ideal, because it does not accompany EOT increase. However, increase of nitrogen concentration seriously degrades NBTI lifetime of PMOSFET and J_g, which are hardly acceptable. On the other hand, comparing PNA and BO, tuning of PNA seems to be reasonable because ΔEOT is smaller. Indeed, increase of d_{opt} with minimizing I_{ds} degradation is achieved by adjusting PNA condition, as shown in Fig.7. From these results, it is confirmed that tuning of PNA condition is effective to fulfill the d_{opt} criteria with maintaining other performance parameters.

To examine why the optical thickness is a good measure of the extrinsic defects, we investigated the physical insight of it and its correlation to defect density. According to our elaborate investigation, the d_{opt} of SiON film is approximately proportional to the area density of atoms in the film, A_{atom}, regardless of nitrogen concentration, as follows.

$$d_{opt} \cong A_{atom} \times 1.46 \times 10^{-23} cm^3. \quad (1)$$

If we introduce a virtual square lattice consisting of unit cells of a single kind similarly in the TDDB modeling as shown by Fig.8, the number of vertically-aligned cells, N, is proportional to d_{opt}, and is given by

$$N = A_{atom} a^2 = d_{opt} a^2 \times 6.85 \times 10^{22} cm^{-3}, \quad (2)$$

where we assumed that the lattice constant parallel to the Si substrate, a, is equal to that of a virtual cubic lattice of SiON. For d_{opt}=1.7nm, N is estimated to be 7. Based on the percolation theory, the probability that a vertical array of cells becomes conductive, P, is calculated as

$$P = \sum_{i=N-N_{th}}^{N} {}_N C_i \, p^i (1-p)^{N-i} \quad , \qquad (3)$$

where p is the fraction of defective cells and we assumed that the array becomes conductive even when some of the cells are normal. N_{th} is the threshold number of normal cells when the array begins to be conductive. Note that N_{th} is 0 in the conventional TDDB theory. Finally the area density of the defects, D_{def}, is obtained as a function of d_{opt} or N by

$$D_{def} = \frac{P}{a^2} \quad . \qquad (4)$$

Therefore, d_{opt} is a good measure of the extrinsic defect and control of it is critical to maintain low defect density.

Fig.9 comparatively shows the experimental results by black dots based on the data of Fig.5 and calculated results by curves, respectively. In the calculation, we added a constant, D_{def0}, to the result by Equation (4), which is attributed to the V_{ddmin}-failures caused by other than leakage current in the gate insulators. The calculation agrees best with the experiment when we assume N_{th} to be 3 or 4. p was 1.1×10^{-4} and 5.0×10^{-6} for N_{th}=3 and 4, respectively.

3. Conclusions

By measuring the minimum supply voltage (V_{ddmin}) for normal operation of logic test RAMs, we successfully detected extrinsic defects including minute breakdown (I_g~μA) built in the ultra thin SiON gate insulators for 65nm node CMOSFETs. It was found that the defect density correlates weakly with J_{gn} or EOT but strongly with the ellipsometrically measured optical thickness (d_{opt}). In order to maintain the low defect density of ultra thin SiON gate insulator in consideration of mass production, the process condition control satisfying d_{opt} >~1.7nm is very important. In order to fulfill this criterion, optimization of PNA condition is effective. Furthermore, by applying the percolation theory, we found that the leakage current paths (extrinsic defects) were generated even when 3 or 4 in 7 cells were defective.

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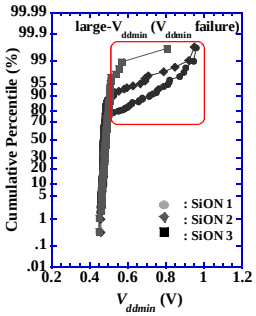

Fig1. Cumulative distribution of V_{ddmin} of test RAMs.

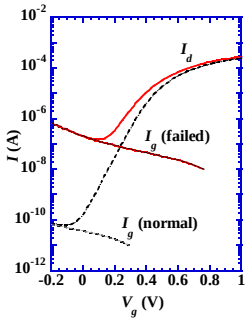

Fig2. I_d-V_g curve by using a nanoprober. MOSFET gate leakage current of a fail bit shows abnormal increase to ~μA range.

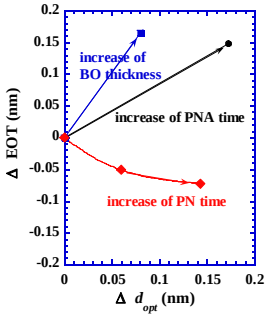

Fig6. Δd_{opt} vs. ΔEOT by changing the PN, PNA and BO process conditions.

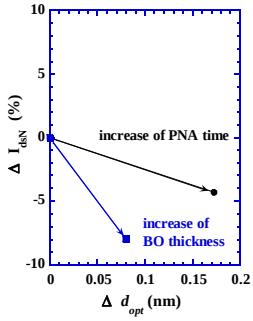

Fig7. Δd_{opt} vs. ΔI_{dsN} by changing the PN and PNA process conditions.

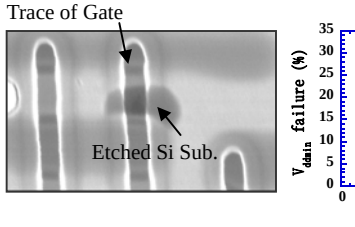

Fig3. SEM image of a failed bit observed after selectively etching off the gate electrodes.

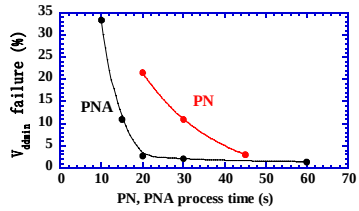

Fig4. Fraction of V_{ddmin}-failure as a function of process time of PN and PNA.

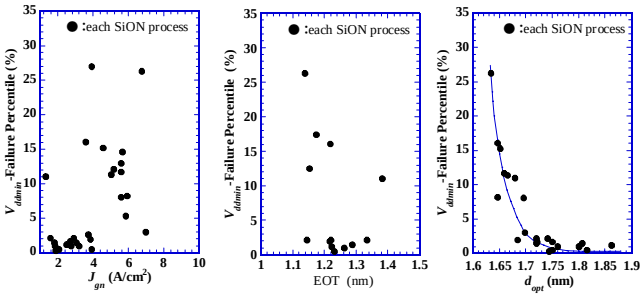

Fig5. Fraction of V_{ddmin}-failure as a function of gate leakage current of NMOSFET (J_{gn}), EOT and d_{opt}.

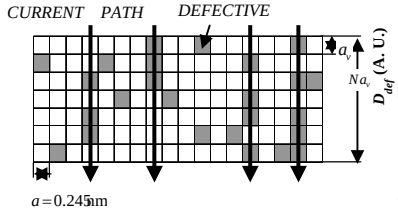

Fig8. Model of breakdown defects in the ultra thin gate insulator.

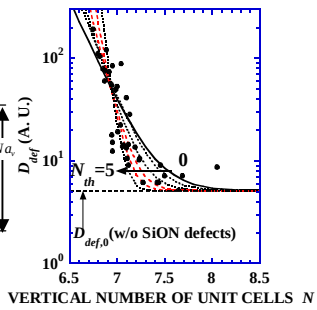

Fig9. Comparison of defect density by experiment and calculation.