Development of high-k / metal gate CMOS technology in Selete

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1. Introduction

Semiconductor leading edge technologies, Inc. (Selete)

Selete was initiated in Feb. 1996 as a purely private sector consortium for developing 300-mm wafer-based production technologies. Under the Asuka Project, launched in 2001, Selete constructed an integrated CMOS line and engaged in the development of hp45nm module technologies.

In April 2006, Selete began a new 5-year program to take part in the Asuka II project, in collaboration with the semiconductor industry and the MIRAI Project commissioned by NEDO. In these programs, we are developing hp45/32nm-compatible module technologies.

2. Development of high-k / metal gate CMOS technology in Selete

2.1. Control with element-incorporated high-k

In 2006, when the present FEP program started, it had been clarified that the Vth-control by the DM with two values of work function (WF) is difficult in the gate first CMOS fabrication procedure, in which the HK/MG stack is exposed to high-temperature S/D activation annealing. Thus, same time DM approach has still been continued. However, the Vth (Vib) modulation technique by incorporating elements into high-k films were actively reported [1-4]. Selete also has started the process development, using the element incorporation method, while we improved our DM technology, as shown in Fig. 1(a). Through the latter, and the dual high-k (DHK) technology, we reported the method whereby Al is incorporated into the high-k film from the WF-metal including Al, which is currently used for the PMOS-highk as standard (Fig. 4 and Fig. 5) [7]. A similar method, employing Mo/AlN electrodes, was reported in the same meeting [8].

At the same time, we started the process development of the method [1, 3, 4] which incorporates the elements from the cap layer into the high-k film. In the first step of this development, we compared the Vfb modulation efficiency between the cap materials, as did other groups. For this work, we developed the ALD method for ultra-thin cap film deposition, as shown in Fig. 6-9. The rapid startup of our ALD technique with the thin film thickness controllability was able to contribute to our smooth progress of the CMOS integration development.

It is significant to reveal the influence on device reliability when the capping method is applied to DHK CMOS. We have evaluated the reliability of the devices that indicate satisfactorily stable electrical properties. Through this work, we clarified the reliability improvement with Vth control element incorporation into high-k films. Moreover, we discussed the mechanism of the improvement. This work was performed in cooperation with “High-k Net” to be described below (Fig. 9-11) [11, 12].

Proposal and development of single-metal/dual-high-k CMOS

As mentioned above, Vth control techniques used for the gate-first CMOS integration have changed from those employing the work functions of the DM electrodes to those that employ the effective work functions of the DHK. In this technology transition, we proposed the single-metal/dual-high-k (SM/DHK) CMOS integration as the best solution for the practical use and production (Fig. 12 and Fig. 13) [13]. This seems to be the first time that such a proposal was mooted, using the very term, at an academic meeting. Of course, it is probable that most of the other groups also had investigated a similar type of integration. However, at the same time, other publications still reported on DM CMOS integration and the improvement of the Vfb control by the element-incorporated high-k for either NMOS or PMOS, separately. In our proposal, the gate structure has a single TiN metal as the electrode, with Mg incorporated high-k for NMOS and Al incorporated high-k for PMOS. This structure is the model that is now being developed in the final phase for production.

In 2008, gate first SM/DHK CMOS integration became the main technology, and this, rather than DM, was reported at academic meetings [14, 15]. We also started the development of the SM/DHK CMOS integration as the productive technology for hp32nm devices. As part of our work, we have been making comparisons between a number of promising candidates for CMOS integration procedure. At the same time, we started the process development of the SM/DHK technology, and this, rather than DM, was reported at academic meetings [1-4, 8]. We also started the development of the SM/DHK CMOS technology, and this, rather than DM, was reported at academic meetings [1-4, 8].

3. Conclusion

The development of the HK/MG CMOS technology in the Selete program, from year to year, was introduced. It is a matter of pride that we lead, or acted a part in, the progress of the development of the gate first SM/DHK technology, as one of the key HK/MG CMOS integration technologies.

References

Fig.1 Dual metal CMOS technology by using RSSL method [5].

Fig.2 Schematic cross-section of dual-metal (DM) gate process flow [6].

Fig.4 After dual-metal/single-high-k (DM/SHK) gate stack is fabricated, Al atoms of Al-containing WFM (p-MOS WFM) are incorporated into HfSiON by high temperature anneal [7].

Fig.7 Sub-threshold characteristics when the ALD-La2O3 caps are applied [10].

Fig.8 Ion-Ioff characteristics with ALD-La2O3 cap layers [10].

Fig.10 Weibull distribution of Tbd with La incorporation [12].

Fig.11 The difference in the electron trap levels between HiOx and HiLaOx is 0.5 eV [12].

Fig.13 Id-Vg curves for Lg=100 nm with and without MgO or AlOx [13].

Fig.14 TEM cross-sectional views of n- and p-MOS FETs fabricated by using our cost-conscious CMOS integration procedure [16].

Fig.15 Dependence of ΔVth on PCA temperature for n and pMOS [16].

Fig.16 C-V curves of HfSiON nFETs with poly-Si/WFM-TiN gates [18].

Fig.17 Vth and EOT of HfSiON nFETs as a function of the WFM-TiN thickness [18].

Fig.18 Guidelines for optimum metal gate structures. A Si-containing layer such as poly-Si and TaSiN on thin WFM (0–4 nm) acts as a WF-lowering layer in nFETs [18].