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Development of high-k / metal gate CMOS technology in Selete

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1. Introduction

Semiconductor leading edge technologies, Inc. (Selete)

Selete was initiated in Feb. 1996 as a purely private sector consortium for developing 300-mm wafer-based production technologies. Under the Asuka Project, launched in 2001, Selete constructed an integrated CMOS line and engaged in the development of hp65nm module technologies.

In April 2006, Selete began a new 5-year program to take part in the Asuka II project, in collaboration with the semiconductor industry and the MIRAI Project commissioned by NEDO. In these programs, we are developing hp45/32nm-compatible module technologies.

Front End Process (FEP) program

The front-end process program was initiated in Apr. 2006 for the development of high-k / metal gate (HK/MG) stack technology, aiming for practical use at the hp45/32nm nodes. The target is to establish technology for HK/MG CMOS processing and reliability. For this purpose, we also examines the technology which has been transferred from the MIRAI Project (second phase) as a part of their result.

In the 2005 fiscal year, before the present FEP program started, we had already developed HK/MG stack technologies corresponding to the hp45nm technology nodes. In this work, we achieved the development of the high-k film that has the properties, sufficient to satisfy the demands of hp45nm devices. While using this high-k, we also developed the W gate-electrode dual-metal/single-high-k (DM/SHK) CMOS technology. In 2006 and 2007FY, we focused on the establishment of HK/MG CMOS technology for hp45nm. In 2008FY, we have focused on the establishment of HK/MG CMOS base-technology for hp32nm. We compared several possible CMOS fabrication procedures, based on MOSFET electrical characteristics, reliability, and the difficulties of the dual high-k (DHK) integration and the ultra-fine gate-stack fabrication. We also made an effort to define the guide-lines for the improvement of reliability. In 2009FY, as our final year, we are working on the development of the CMOS module technologies with more refined integration and processes.

2. Development of high-k / metal gate CMOS technology in Selete

Vth control with element-incorporated high-k

In 2006, when the present FEP program started, it had been clarified that the Vth-control by the DM with two values of work function (WF) is difficult in the gate first CMOS fabrication procedure, in which the HK/MG stack is exposed to high-temperature S/D activation annealing. At the same time, the DM approach had still been continued. However, the Vth (Vfb) modulation technique by incorporating elements into high-k films were actively reported [1-4]. Selete had also started the process development, using the element incorporation method, while we improved our DM technology, as shown in Fig. 1-3 [5, 6]. Through the latter, as the dual high-k (DHK) technology, we reported the method whereby Al is incorporated into the high-k from the WF-metal including Al, which is currently used for the PMOS-high-k as standard (Fig. 4 and Fig. 5) [7]. A similar method, employing MoAlN electrodes, was reported in the same meeting [8].

At the same time, we started the process development of the method [1, 3, 4] which incorporates the elements from the cap layer into the high-k film. In the first step of this development, we compared the Vfb modulation efficiency between the cap materials, as did other groups. For this work, we developed the ALD method for ultra-thin cap film deposition, as shown in Fig. 6-8 [9, 10]. The rapid startup of our ALD technique with the thin film thickness controllability was able to contribute to our smooth progress of the CMOS integration development.

It is significant to reveal the influence on device reliability when the capping method is applied to DHK CMOS. We have evaluated the reliability of the devices that indicate satisfactorily stable electrical properties. Through this work, we clarified the reliability improvement with Vth control element incorporation into high-k films. Moreover, we discussed the mechanism of the improvement. This work was performed in cooperation with "High-k Net" to be described below (Fig. 9-11) [11, 12].

Proposal and development of single-metal/dual-high-k CMOS

As mentioned above, Vth control techniques used for the gate-first CMOS integration have changed from those employing the work functions of the DM electrodes to those that employ the effective work functions of the DHK. In this technology transition, we proposed the single-metal/dual-high-k (SM/DHK) CMOS integration as the best solution for the practical use and production (Fig. 12 and Fig. 13) [13]. This seems to be the first time that such a proposal was mooted, using the very term, at an academic meeting. Of course, it is probable that most of the other groups also had investigated a similar type of integration. However, at the same time, other publications still reported on DM CMOS integration and the improvement of the Vfb control by the element-incorporated high-k for either NMOS or PMOS, separately. In our proposal, the gate structure has a single TiN metal as the electrode, with Mg incorporated high-k for NMOS and Al incorporated high-k for PMOS. This structure is the model that is now being developed in the final phase for production.

In 2008, gate first SM/DHK CMOS integration became the main technology, and this, rather than DM, was reported at academic meetings [14, 15]. We also started the development of the SM/DHK CMOS integration as the productive technology for hp32nm devices. As part of our work, we have been making comparisons between a number of promising candidates for CMOS integration procedure. At this SSDM2009, we will report a cost-conscious SM/DHK CMOS integration, as shown in Fig. 14 and Fig. 15 [16]. On the other hand, as the one of the SM integration techniques, we have investigated a different method [17] which can control the effective work function by differing metal thicknesses (Fig. 16-18) [18].

Other developments

As part of our mission, we have investigated as many as possible other materials and processes for suggestion to our clients as candidates, and we have also performed work for the solution of the problems and the optimization of the process for the SM/DHK CMOS integration, described above. For example, in SSDM, we have reported on the Ta system electrode (influence of N [19], CVD[20]), MIFS(FUSI) electrodes [21], high-k process (influence of N [22], ultra-thin EOT[23, 24]), Cap process (annealing for Al2O3-Cap) [25], together with HK/MG FET fabrication process (SW[26], FSP-FLA[27], high temperature S/D annealing[28]).

"High-k Net" activity

In order to apply new materials, such as metal gates and high-k dielectrics, into the practical CMOS process, we require a deep understanding of the scientific aspects of materials and processes. To this end, "High-k Net" has been established as an industry-university collaboration scheme, in which the activities of both sides have been complementarily supported. The activity has been mainly focused on the reliability issue of high-k gate dielectrics and understanding of interfacial phenomena between metal gate and high-k. Some of these activities were presented at international conferences, confirming the high performance of the "High-k Net" collaboration [29-33].

3. Conclusion

The development of HK/MG CMOS technology in the present Selete program, from year to year, was introduced. It is a matter of pride that we lead, or acted a part in, the progress of the development of the gate first SM/DHK technology, as one of the key HK/MG CMOS integration technologies.

References [1] H.N. Alshareef et al., VLSI (2006) 10. [2] S. C. Song et al., VLSI (2006) 16. [3] H-S. Jung et al., VLSI (2006) 204. [4] V. Narayanan et al., VLSI (2006) 224. [5] Y. Akasaka et al., VLSI (2006) 206. [6] F. Ootsuka et al., SSDM (2006) 1116. [7] M. Kadoshima et al., VLSI (2007) 66. [8] H. –C. Wen et al., VLSI (2007) 160. [9] S. Kamiyama et. Al., ALD#7 (2007) 128. [10] S. Kamiyama et al., IEDM (2007) 539. [11] M. Sato et al., VLSI (2008) 66. [12] M. Sato et al., IEDM (2008) 119. [13] N. Mise et al., IEDM (2007) 527. [14] X. Chen et al., VLSI (2008) 88. [15] T. Schram et al., VLSI (2008) 44. [16] H. Shinohara et al., SSDM (2009). [17] H-S. Jung et al., VLSI (2007) 196. [18] M. Kadoshima et al., VLSI (2008) 48. [19] T. Onizawa et al., SSDM (2007) 248. [20] Y. Sugita et al., SSDM (2008) 854. [21] M. Kadoshima et al., SSDM (2008) 846. [22] T. Matsuki et al., SSDM (2006) 410. [23] D. Ishikawa et al., SSDM (2007) 846. [24] D. Ishikawa et al., SSDM (2008) 858. [25] T. Morooka et al., SSDM (2008) 24. [26] N. Mise et al., SSDM (2007) 724. [27] T. Onizawa et al., SSDM (2008) 844. [28] M. Sato et al., SSDM (2008) 20. [29] N. Umezawa et al., SSDM (2006) 460. [30] Z. Ming et al., SSDM (2006) 380. [31] K. Shiraishi et al., SSDM (2007) 844. [32] K. Ohmori et al., IEDM (2007) 345. [33] J. Chen et al., SSDM (2008) 356.

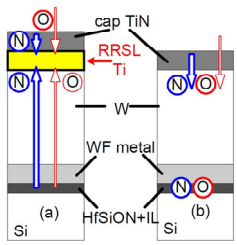

Fig.1 Dual metal CMOS technology by using RRSL method [5].

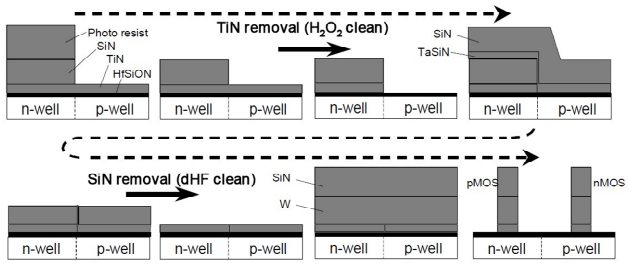

Fig.2 Schematic cross-section of dual-metal (DM) gate process flow [6].

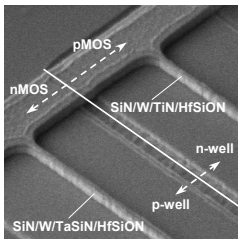

Fig.3 SEM view of W/TiN/HfSiON and W/TaSiN/HfSiON gate stacks [6].

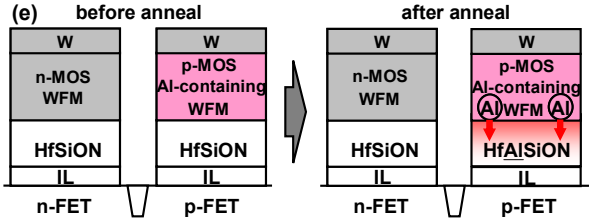

Fig.4 After dual-metal/single-high-k (DM/SHK) gate stack is fabricated, Al atoms of Al-containing WFM (p-MOS WFM) are incorporated into HfSiON by high temperature anneal [7].

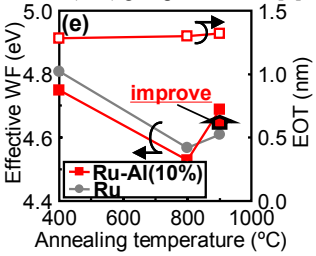

Fig.5 Effective WF of Al-containing WFM on HfSiON [7].

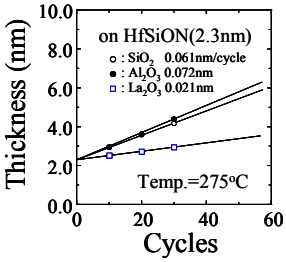

Fig.6 Thickness of ALD as a function of the number of the growth cycles [9].

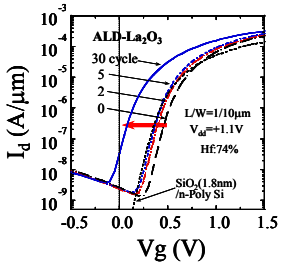

Fig.7 Sub-threshold characteristics when the ALD-La_2O_3 caps are applied [10].

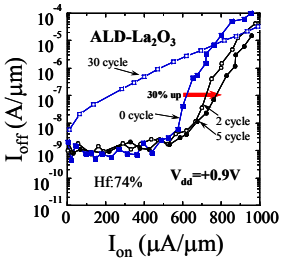

Fig.8 Ion-Ioff characteristics with ALD-La_2O_3 cap layers [10].

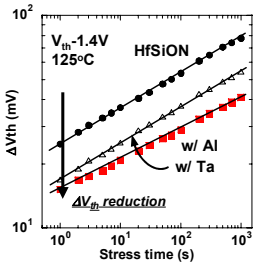

Fig.9 Time evolution of ΔVth in NBTI [11].

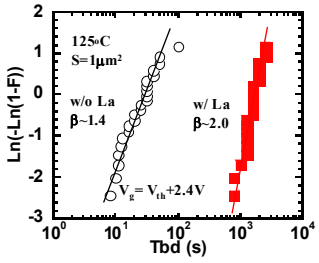

Fig.10 Weibull distribution of Tbd with La incorporation [12].

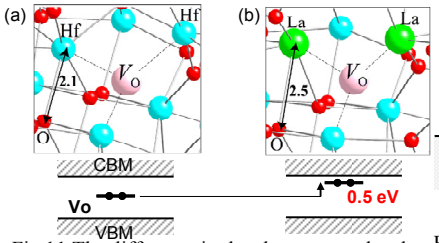

Fig.11 The difference in the electron trap levels between HfOx and HfLaOx is 0.5 eV [12].

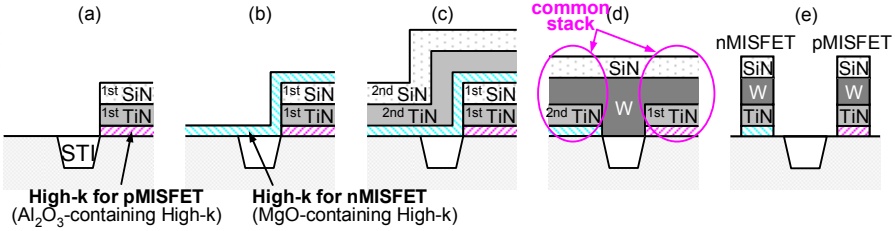

Fig.12 Main process steps for single-metal/dual-high-k (SM/DHK) gate stack including (a) Al_2O_3-containig high-k deposition for pMISFET, (b) MgO-containing high-k deposition for nMISFET, (c)-(d) common gate stack formation for nMISFET and pMISFET, and (e) gate definition [13].

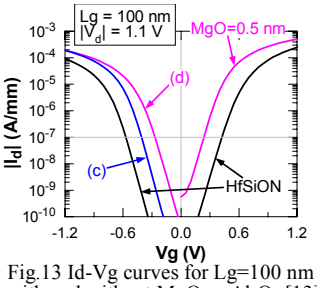

Fig.13 Id-Vg curves for Lg=100 nm with and without MgO or Al_2O_3 [13].

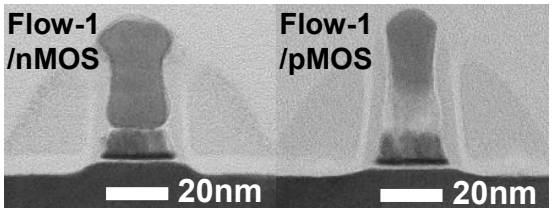

Fig.14 TEM cross-sectional views of n- and p-MOS FETs fabricated by using our cost-conscious CMOS integration procedure [16].

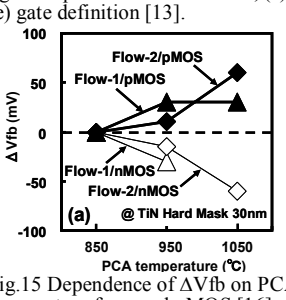

Fig.15 Dependence of ΔVfb on PCA temperature for n and pMOS [16].

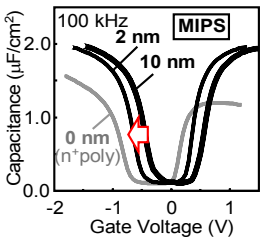

Fig.16 C-V curves of HfSiON nFETs with poly-Si/WFM-TiN gates [18].

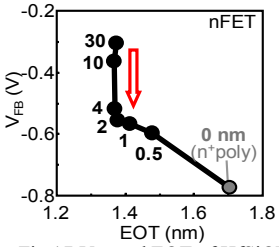

Fig.17 V_{FB} and EOT of HfSiON nFETs as a function of the WFM -TiN thickness [18].

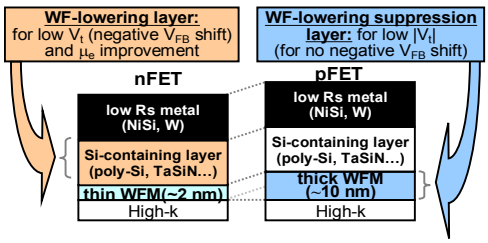

Fig.18 Guidelines for optimum metal gate structures. A Si-containing layer such as poly-Si and TaSiN on thin WFM (0~4 nm) acts as a WF-lowering layer in nFETs [18].