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Gate Leakage Advantage of LaO Incorporation for V_t Tuning in High-k nMOSFETs over Metal Gate WF Control

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Abstract We have investigated impacts of LaO incorporation into a high-k dielectric (HK) for threshold voltage (V_t) tuning on gate leakage current (J_g) in HK nFETs in detail. A J_g-V_g curve is not shifted along with a change in V_t and J_g decreases at fixed V_g when V_t is decreased by LaO incorporation in HK nFETs. Evaluation of barrier heights at a metal gate (MG)/HK interface suggests that this is owing to no decrease of the conduction band offset at a MG/HK interface by LaO incorporation. On the other hand, J_g increases at fixed V_g because a J_g-V_g curve is shifted along with V_t when a work-function (WF) is lowered by MG. Therefore, a V_t tuning technique of LaO incorporation has a clear advantage over a WF control by MG for suppressing the J_g increase associated with the continued scaling of CMOSFETs.

1. Introduction

The biggest merit of replacing a conventional poly-Si/SiON gate stack with a MG/HK gate stack is suppression of a J_g increase in scaled CMOS. That brings the benefits of miniaturization of CMOSFETs to us as before. When we use a MG/HK gate stack in CMOSFETs, high V_ts are one of serious problems. LaO incorporation into HK is effective to reduce V_t in HK nFETs [1-5]. A mechanism of the V_t shift, namely the effective WF shift of MG by LaO-incorporation has been extensively studied. The interface between HK and SiO_2 interface layer (IL) plays an important role in the effective WF shift. It is considered that a local potential drop forms due to interface dipoles at the interface [2-3,5]. However, impacts of LaO incorporation into HK on J_g in HK nFETs have rarely been reported. In this study, we focus on changes in J_g characteristics by LaO incorporation into HK. It will be shown that LaO incorporation is effective not only for decreasing V_t but also for suppressing a J_g increase.

2. Experimental

Gate-first LaO-incorporated Hf-based HK n and pFETs with poly-Si/TiN gate electrodes were investigated. EOTs of the gate dielectric were approximately 1.3 nm. TiN and CVD-poly-Si layers were deposited on HK. HK nFETs with three different TiN thicknesses were also evaluated.

3. Results and Discussion

I_d-V_g curves for both HK n and pFETs are shifted by approximately 0.3 V towards the negative V_g direction after LaO incorporation (**Fig. 1**). Apparently, a J_g-V_g curve of the HK pFET seems to be shifted towards the negative V_g direction along with the I_d-V_g shift. However, judging from the difference between a shift in J_g-V_g and a shift in I_d-V_g in the HK nFETs, we should consider that J_g values are decreased by LaO incorporation for both the HK FETs as shown by arrows in **Fig. 1**.

Based on the studies on effective WF shifts by LaO incorporation into HK [2-3,5], an effective WF of MG is effectively modulated at the interface between HK and SiO_2 interface layer (IL) (**Fig. 2**). The modulation at the HK/IL interface hardly changes the conduction band offset (ϕ_b) at the MG/HK interface except for a change in band gap of HK by LaO incorporation (**Fig. 2**). Therefore, J_g-V_g characteristics are expected to remain almost unchanged after LaO incorporation.

Here, we investigate the validity of the above consideration by evaluating a change in ϕ_b by LaO incorporation. We estimate ϕ_b at a MG/HK interface by a simple method proposed by S. Zafar *et al* [6]. This is based on the fact that the carrier transport mechanism changes from direct tunneling (DT) to Fowler-Nordheim (FN) tunneling at $V_g=\phi_b/q$ (**Fig. 3**), if J_g is limited by a tunneling event and mainly consists of electron current from channel to MG in nFETs. Since tunneling probability is changed at $V_g=\phi_b/q$, $d\ln(J_g)/dV_g$ shows a peak at the point of $V_g=\phi_b/q$.

Actually, it is confirmed that electron current from the Si channel is predominant in J_g of the HK nFETs (**Fig. 4**) and the carrier transport mechanism is tunneling because temperature dependence of J_g is negligible. ϕ_b for HK without LaO is estimated to be 1.50 eV, that is very close to a calculated ϕ_b for Hf-based HK (**Fig. 4**) [7]. Roughly estimated ϕ_b from FN-plot shows the similar trend (**Fig. 5**).

A slight ϕ_b increase, namely no ϕ_b decrease is observed after LaO incorporation in the HK nFETs (**Fig. 4**). This suggests that the above-mentioned model is valid. The slight ϕ_b increase must be due to a change in band gap of bulk HK because ϕ_b of LaO is larger than that of Hf-based HK [7]. J_g is decreased by the ϕ_b increase and by a total thickness increase of HK and IL (**Fig. 6**) after LaO incorporation.

ϕ_b shifts are also evaluated when V_t is controlled by changing the TiN thickness in poly-Si/TiN gate electrodes for comparison (**Fig. 7**). In this case, an effective WF of TiN is modulated at a MG(TiN)/HK interface (**Fig. 8**) [8]. It can be seen that the J_g–V_g characteristics are shifted along with V_t (**Figs. 7 and 9**). Both ϕ_b and V_t are decreased with decreasing the TiN thickness (open circles in **Fig. 10**). The impacts of (i) LaO incorporation and (ii) a change in the TiN thickness on ϕ_b, are totally different (**Fig. 10**).

J_g at V_g=1.1V actually decreases after LaO incorporation, while J_g at V_g=1.1V increases with decreasing V_t by decreasing the TiN thickness (**Fig. 11**). This is owing to no shift in a J_g-V_g curve towards the negative V_g direction (**Fig. 12**) and an increase in a total physical thickness of a gate dielectric (**Figs. 1 and 6**). Thus, LaO incorporation should be intentionally used for obtaining not only low V_t but also low J_g in HK nFETs. Similarly to LaO incorporation in HK nFETs, J_g is decreased by AlO incorporation in HK pFETs thanks to no J_g-V_g shift (**Fig. 13**). Moreover, ϕ_b increases after AlO incorporation into HK owing to the large band-gap of AlO (**Fig. 13**) [7].

4. Conclusion

Impacts of a V_t tuning technique of LaO incorporation into HK on J_g of nFETs have been studied in detail. It is clearly shown that J_g-V_g characteristics are hardly shifted along with V_t by LaO incorporation, but are shifted by WF control of MG such as a decrease of a TiN thickness in MG. Therefore, LaO incorporation for V_t tuning is superior to WF control techniques by MG with respect to suppressing the J_g increase in scaled CMOSFETs.

References

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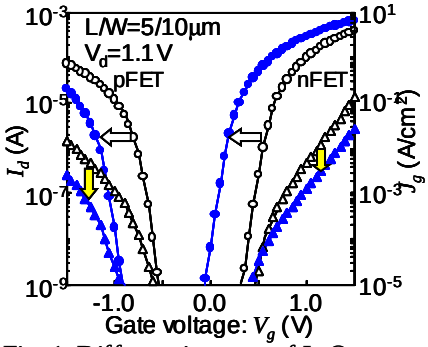

Fig. 1 Different impacts of LaO incorporation into HK on I_d-V_g (circles) and J_g-V_g (triangles). Solid and open symbols indicate the results of HK FETs with and w/o LaO, respectively.

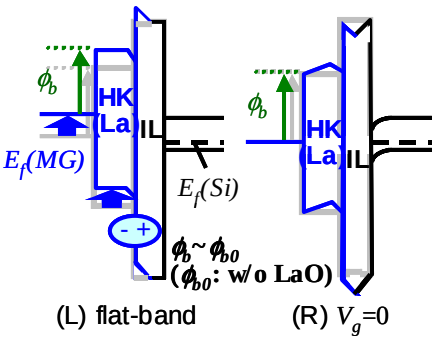

Fig. 2 Expected band diagrams (L) at flat-band and (R) at V_g=0 of a MG/LaO-incorporated HK gate stack. While E_f of MG is effectively shifted upwards, ϕ_b is almost unchanged.

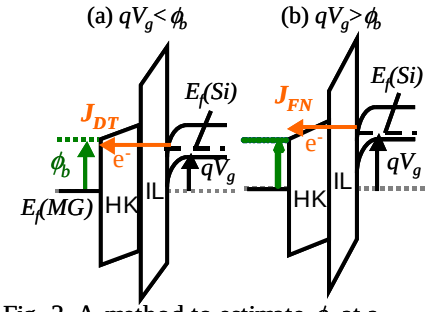

Fig. 3 A method to estimate ϕ_b at a MG/HK interface. If J_g of HK nFETs in strong inversion is mainly determined by electron tunneling from the channel, the tunneling mechanism changes from (a) DT to (b) FN tunneling at V_g=ϕ_b/q.

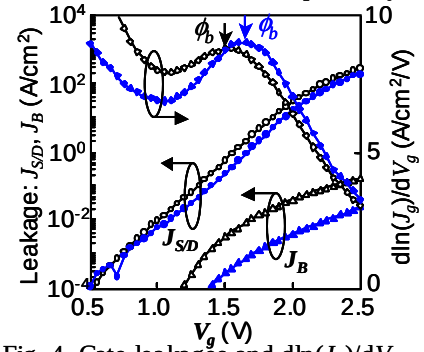

Fig. 4 Gate leakages and dln(J_g)/dV_g for HK nFETs with (solid) and w/o LaO (open symbols). ϕ_b remains almost unchanged irrespective of LaO-incorporation into HK.

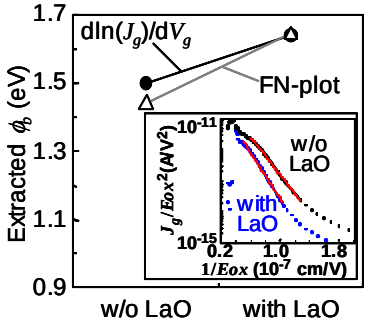

Fig. 5 ϕ_bs extracted by dln(J_g)/dV_g (Fig. 4) and FN-plot (inset). Changes in both extracted ϕ_b by LaO-incorporation are small.

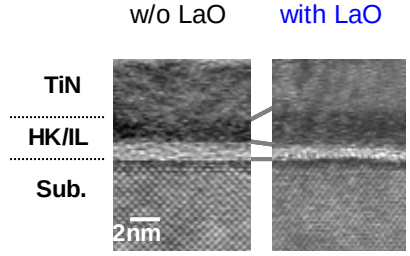

Fig. 6 Cross-sectional TEM images of TiN/HK/IL/Si-sub. structures w/o (left) and with LaO (right). The total physical thickness of HK/IL with LaO is thicker than that of HK/IL without LaO.

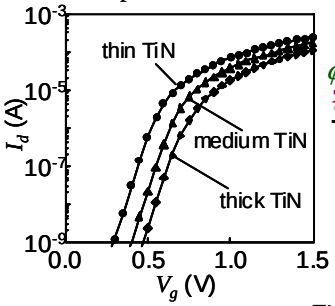

Fig. 7 I_d-V_g curves of poly-Si/TiN/HK nFETs. V_t decreases with decreasing the TiN thickness.

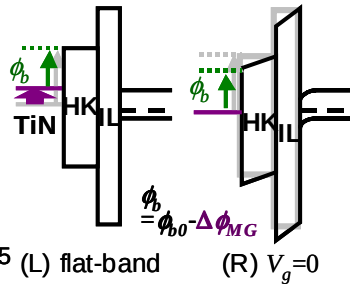

Fig. 8 Band diagrams (L) at flat-band and (R) at V_g=0 of TiN/HK gate stacks when changing the TiN thickness. ϕ_b is reduced as shown by an arrow along with a decrease of WF of MG.

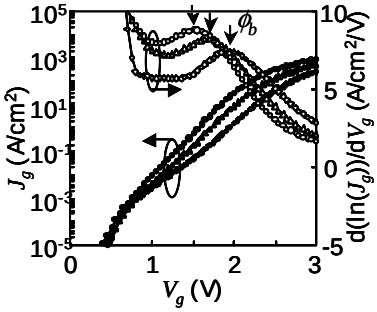

Fig. 9 J_g and dln(J_g)/dV_g of HK nFETs with thin- (circles), medium- (triangles), or thick-TiN (diamonds). ϕ_b is shifted positively with increasing V_t.

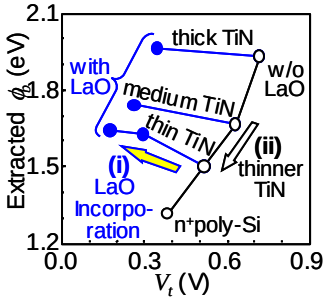

Fig. 10 ϕ_b vs. V_t of HK nFETs. Impacts of (i) LaO incorporation and (ii) a change in TiN thickness for V_t tuning on ϕ_b are totally different.

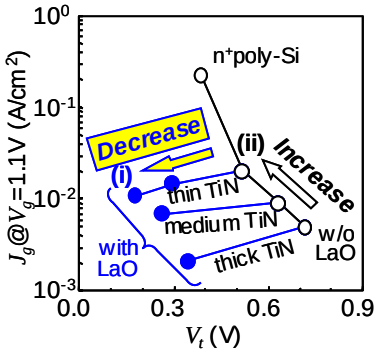

Fig. 11 J_g of HK nFETs. V_t is controlled by (i) LaO-incorporation and (ii) TiN thickness modulation. J_g increase is suppressed by (i) LaO incorporation.

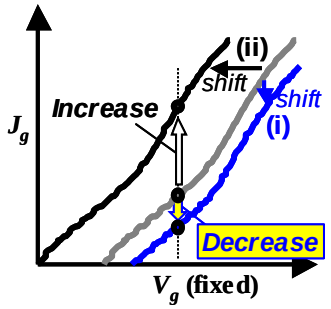

Fig. 12 Schematics of impacts on J_g when using (i) and (ii) for obtaining low V_t. J_g is shifted towards the (i) lower J_g and (ii) negative V_g directions. J_g at fixed V_g such as V_{dd} is decreased by (i), but is increased by (ii).

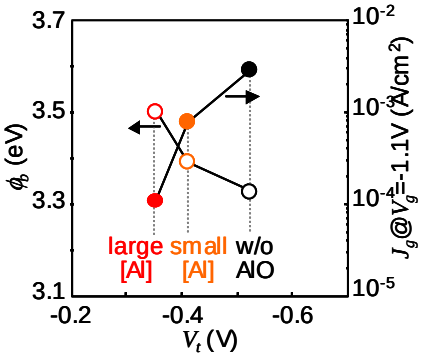

Fig. 13 Estimated ϕ_b and measured J_g as a function of V_t of HK pFETs. ϕ_b increases with decreasing $|V_t|$ by AlO-incorporation into HK. Thus, J_g decreases at a fixed V_g.