Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp785-786

Bottom-La Inserted HfSiON Gate Dielectrics with MOCVD HfCN Metal Gate Electrode Realizing High Mobility and Reliability Improvement

S. Inumiya, A. Kaneko, K. Nagatomo*, M. Goto*, K. Tatsumura**, I. Hirano**, S. Kawanaka*, A. Azuma*, K. Nakajima, T. Aoyama, K. Eguchi, A. Nishiyama**, Y. Toyoshima* and Y. Tsunashima
Process & Manufacturing Engineering Center, *Center for Semiconductor Research & Development, Semiconductor Company, **Advanced Semiconductor Laboratory, Research & Development Center, Toshiba Corporation
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Tel +81-45-776-5418, Fax +81-45-776-4106, E-mail: seiji.inumiya@toshiba.co.jp

1. Introduction

An introduction of HK/MG into gate-first CMOS device is strongly required to meet a requirement of ultra-short gate length in 28nm node and beyond. Recently, La-cap process [1, 2] is frequently used as an EWF tuning process for Hf-based HK/MG nMOS and the EWF modulation has been revealed to be originated from La-induced dipoles at HK/SiO_2 interface [3]. Since the V_{fb} or V_{th} shift is ruled by the amount of La atoms diffused through HK layer, the La-cap process seems to be quite a high-k layer sensitive process. Although a process of La(O)-cap "below" high-k (HfSiO) with a laser annealing [4, 5] has been proposed, its stability under a conventional high temperature spike annealing have not been clarified yet. Besides, La induces k-value enhancement makes T_{inv} mismatch between nMOS and pMOS large. This is another issue for La incorporation process.

In this work, a direct insertion of La into a thermally stable ultra-thin HfSiON [6]/IL (named bottom-La hereafter) was evaluated to achieve a robust V_{th} controllability. The bottom-La inserted HfSiON showed high electron mobility and reliability improvements, with newly developed MOCVD HfCN gate electrode which can reduce T_{inv} in pMOS.

2. Experimental

Figure 1(a) shows process flow and stack structure of bottom-La inserted HfSiON gate dielectrics. Prior to $HfSiO_x$ deposition, La was deposited directly on interfacial layer. Then, $HfSiO_x$ was deposited by MOCVD using TDEAH, TDMAS and oxygen followed by plasma nitridation and post nitridation annealing. La-capped (top-La) HfSiON (Fig. 1(b)) were also fabricated for comparison. To evaluate V_{fb}, EOT and J_g, MOS capacitors were fabricated using TaC-MIPS and Ni-FUSI gate electrode. HfCN films were deposited by MOCVD with TDEAH as a precursor. With the HfCN films, MIPS-gate MOSFETs were fabricated using a conventional gate-first CMOS process. A spike annealing at a temperature of above 1050°C was performed for all devices.

3. Results and Discussions

A. Bottom-La Insertion into HfSiON/SiO_2 Interface

Figure 2 shows V_{fb} shift dependence on La thickness in top-La process. The V_{fb} shifts caused by top-La strongly depend on the $HfSiO_x$ thickness, [N] and Hf/(Hf+Si). This means that the V_{fb} shifts are unstable against high-k process fluctuations and cannot be controlled by deposited La thickness only. On the contrary, V_{fb} shifts are almost independent of the [N] and thickness of HfSiON, in the case of direct insertion of bottom-La, as is shown in Fig. 3. V_{fb} shifts of more than 400mV are obtained by only 0.3nm-thick bottom-La insertion. In addition to the V_{fb} shifts, remarkable EOT reductions up to 0.17nm are obtained as shown in Fig. 4. HR-RBS measurement (Fig. 5) revealed that the majority of La atoms stayed in the HfSiON/SiO_2 interface to form the dipoles and some interaction with SiO_2 IFL and HfSiON might occur to reduce the EOT. Fig. 6 shows J_g–T_{eff} relationship of bottom-La inserted HfSiON at positive gate bias. Thanks to the EOT reduction and the drastic reduction of gate leakage current, scalability of HfSiON is improved and becomes to meet the ITRS 28nm (in 2011) targets. The V_{fb} shift by La incorporation is understood to be originated from the dipole induced band-alignment modulation, which brings barrier-height enhancement for electron tunneling [7].

B. MOCVD HfCN Metal Gate Electrode

Figure 7(a) and 7(b) show electron and hole mobility in HfCN/HfSiON (w/o bottom-La), respectively. The thickness of HfSiON and HfCN has no impact on the mobility and the comparative values to poly-Si/HfSiON gate stack [6] are obtained. This means that the MOCVD HfCN realizes damage-less metal gate process for HfSiON gate dielectrics. By using the bottom-La process to HfCN/HfSiON gate stacks, nMOS V_{th} were successfully reduced as shown in Fig.8. Figure 9 shows V_{th} distribution with-in 300mm wafers with and without bottom-La insertion. As expected, tight distribution of V_{th} in bottom-La inserted one was obtained, comparative to the V_{th} distribution of HfCN/HfSiON without La incorporation. Figure 10 shows bottom-La thickness dependence of T_{inv} for HfCN gate and EOT for FUSI gate. By comparing the both dependences, we can conclude that T_{inv} for HfCN gate were reduced by HfCN gate in the case of small amount of La incorporation. This T_{inv} reduction is presumably due to the oxygen scavenging effect of HfCN and favorable to pMOS in which La can not be used for T_{inv} scaling.

C. Mobility and Reliability of Bottom-La Inserted HfSiON

Figure 11 shows surface carrier density dependence of electron mobility in HfCN/HfSiON with bottom-La insertion. Some mobility degradations, particularly in low N_s region, were observed for bottom-La inserted samples. However, the trade-off relationship between V_{th} shift and mobility in high N_s region, as shown in Fig. 12, suggests the degradation is not so serious as to cancel the profits from V_{th} reductions. In addition to V_{th} controllability and high-mobility, bottom-La inserted HfSiON shows drastic improvement both in PBTI and TDDB and will meet 10years requirements, as shown in Fig.13 and Fig.14, respectively.

4. Conclusion

We propose the bottom-La inserted HfSiON gate dielectrics with MOCVD HfCN metal gate electrode. By using the bottom-La process, a robust V_{th} controllability can be obtained, without serious mobility degradation. The bottom-La process successfully provides drastic reliability improvements in nMOS. MOCVD HfCN metal gate provides a reduction of T_{inv} mismatch between nMOS and pMOS. This process will be promising for gate-first fabrication of HK/MG CMOS in 28nm node and beyond.

References

[1] V. Narayanan et al., Symp. on VLSI Tech., p.224-225 (2006).
[2] H. N. Alshareef et al., Symp. on VLSI Tech., p.10-11 (2006).
[3] Y. Yamamoto et al., SSDM, p.212-213 (2006).
[4] T. Schram et al., Symp. on VLSI Tech., p.44-45 (2008).
[5] S. Z. Chang et al., Symp. on VLSI Tech., p.62-63 (2008).
[6] S. Inumiya et al., IEDM Tech. Dig., p.25-28 (2005).
[7] C. Y. Kang et al., IEDM Tech. Dig., p.115-118 (2008).

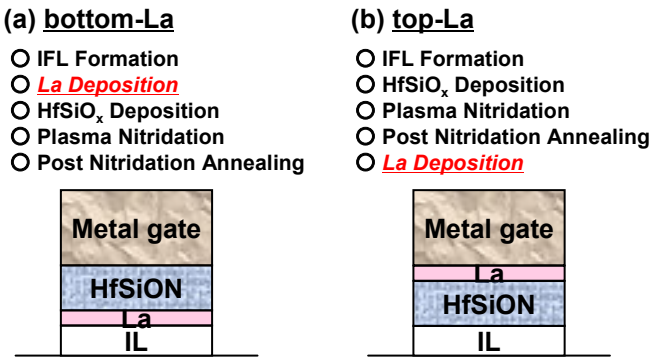

Fig.1 Process flows and stack structures of (a) bottom-La inserted HfSiON and (b) La-capped (top-La) HfSiON. In the case of bottom-La, La is directly placed at the dipole formation position.

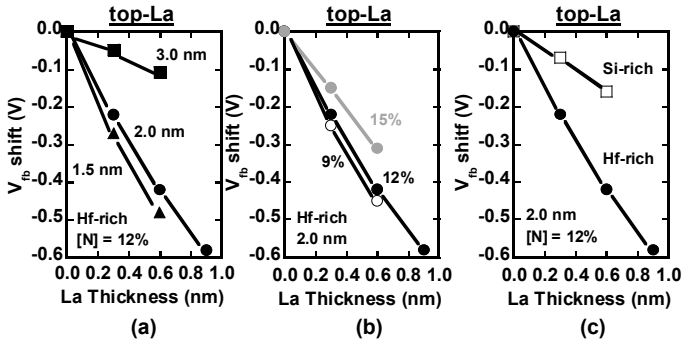

Fig. 2 V_{fb} shift dependence on top-La thickness. (a) deposited $HfSiO_x$ thickness (1.5nnm, 2.0nm, 3.0nm) dependence. (b) nitrogen concentration [N] (9%, 12%, 15%) dependence. (c) Hf/(Hf+Si) (Hf-rich, Si-rich) dependence. TaC MIPS gate was used.

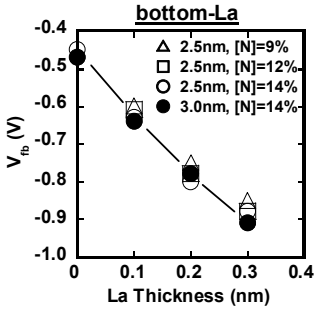

Fig. 3 V_{fb} dependence on inserted bottom-La thickness. Ni-FUSI gate was used. Robust V_{fb} controllability was achieved.

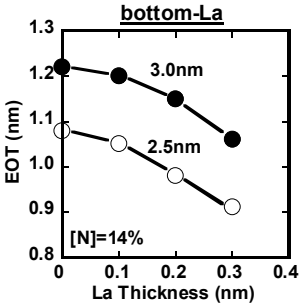

Fig. 4 EOT dependence on inserted bottom-La thickness. Ni-FUSI gate was used.

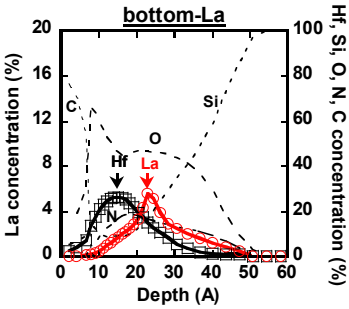

Fig. 5 HR-RBS spectrum of bottom-La inserted HfSiON. 0.3nm thick La was deposited before $HfSiO_x$ deposition.

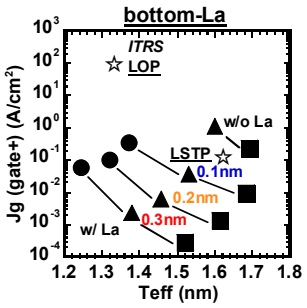

Fig. 6 J_g (gate+)-EOT relationship of HfSiON w/ and w/o bottom-La. Ni-FUSI gte was used. ITRS 28nm LOP and LSTP targets are also shown.

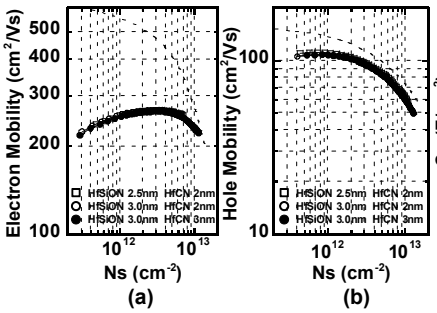

Fig. 7 Surface carrier density dependence of (a) effective electron and (b) effective hole mobility in MOCVD-HfCN/HfSiON gate stacks.

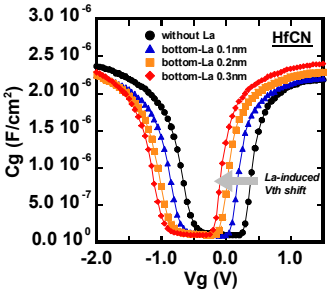

Fig. 8 C-V characteristics of HfCN/HfSiON/SiO_2 gate stack w/ and w/o bottom-La insertion.

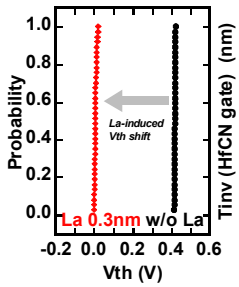

Fig. 9 V_{th} distributions within 300mm wafer for HfCN/HfSiON w/ and w/o bottom-La insertion.

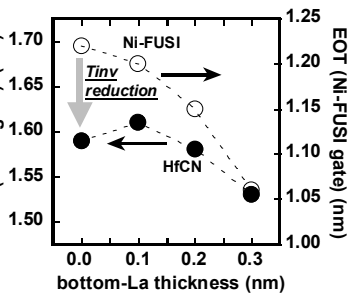

Fig. 10 La thickness dependence of T_{inv}. Turn-around behavior was shown in the case of HfCN gate electrode.

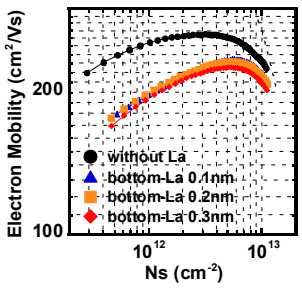

Fig. 11 Surface carrier density dependence of electron effective mobility in HfCN/HfSiON w/ and w/o bottom-La insertion.

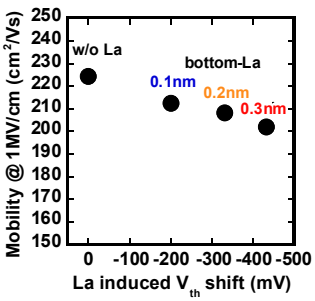

Fig. 12 Trade-off relationship between V_{th} shift and mobility degradation.

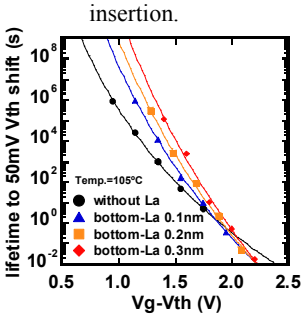

Fig. 13 PBTI characteristics of HfCN/HfSiON nMOS w/ or w/o bottom-La insertion. Drastic improvement was obtained by La incorporation.

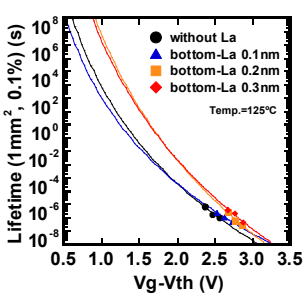

Fig. 14 TDDB characteristics of HfCN/HfSiON nMOS w/ or w/o bottom-La insertion. Drastic improvement was obtained by La incorporation.