**Bottom-La Inserted HfSiON Gate Dielectrics with MOCVD HfCN Metal Gate Electrode Realizing High Mobility and Reliability Improvement**


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1. Introduction

An introduction of HK/MG into gate-first CMOS device is strongly required to meet a requirement of ultra-short gate length in 28nm node and beyond. Recently, La-cap process [1, 2] is frequently used as an EWF tuning process for Hf-based HK/MG nMOS and the EWF modulation has been revealed to be originated from La-induced dipoles at HK/SiO2 interface [3]. Since the Vth or Vfb shift is ruled by the amount of La atoms diffused through HK layer, the La-cap process seems to be quite a high-k layer sensitive process. Although a process of La(O)-cap “below” high-k (HfSiO) with a laser annealing [4, 5] has been proposed, its stability under a conventional high temperature spike annealing have not been clarified yet. Besides, La induces k-value enhancement which can not be compensated by HfCN/HfSiON without La incorporation.

In this work, a direct insertion of La into a thermally stable ultra-thin HfSiO [6] layer was evaluated to achieve a robust Vfb controllability. The bottom-La inserted HfSiON gate dielectrics showed high electron mobility and reliability improvements, with newly deposited MOCVD HfCN metal gate electrode which can reduce Tinv in pMOS.

2. Experimental

Figure 1(a) shows process flow and stack structure of bottom-La inserted HfSiON gate dielectrics. Prior to HfSiOx deposition, La was deposited directly on interfacial layer. Then, HfSiOx was deposited by MOCVD using TDEAH, TDMAS and oxygen followed by plasma nitridation and post nitridation annealing. A-capped (top-La) HfSiON (Fig. 1(b)) were also fabricated for comparison. To evaluate Vth, Vfb and Jg, MOS capacitors were fabricated using TaC-MIPS and Ni-FUSI gate electrode. HfCN films were deposited by MOCVD with TDEAH as a precursor. With the_ _HfCN_ _gate electrode, EOT reductions up to 0.17nm are obtained as shown in Fig. 8. Figure 11 shows Vth distribution of HfCN/HfSiON without La incorporation. Figure 10 shows bottom-La thickness dependence of Tinv for HfCN gate and EOT for FUSI gate. By comparing the both dependences, we can conclude that Tinv for HfCN gate were reduced by HfCN gate in the case of small amount of La incorporation. This Tinv reduction is presumably due to the oxygen scavenging effect of HfCN and favorable to pMOS in which La can not be used for Tinv scaling.

3. Results and Discussions

A. Bottom-La Insertion into HfSiON/SiO2 Interface

Figure 2 shows Vth shift dependence on La thickness in top-La process. The Vth shifts caused by top-La strongly depend on the HfSiOx thickness, [N] and Hf/(Hf+Si). This means that the Vth shifts are unstable against high-k process fluctuations and cannot be controlled by deposited La thickness only. On the contrary, Vth shifts are almost independent of the [N] and thickness of HfSiON, in the case of direct insertion of bottom-La, as is shown in Fig. 3. Vth shifts of more than 400mV are obtained by only 0.3nm-thick bottom-La insertion. In addition to the Vth shifts, remarkable EOT reductions up to 0.17nm are obtained as shown in Fig. 4.

B. MOCVD HfCN Metal Gate Electrode

Figure 7(a) and 7(b) show electron and hole mobility in HfCN/HfSiON (w/o bottom-La), respectively. The thickness of HfSiON and HfCN has no impact on the mobility and the comparative values to poly-Si/HfSiON gate stack [6] are obtained. This means that the MOCVD HfCN realizes damage-less metal gate process for HfSiON gate dielectrics. By using the bottom-La process to HfCN/HfSiON gate stacks, nMOS Vth were successfully reduced as shown in Fig. 8. Figure 9 shows Vth distribution in 300nm wafers with and without bottom-La insertion. As expected, tight distribution of Vth in bottom-La inserted one was obtained, comparative to the Vth distribution of HfCN/HfSiON without La incorporation. Figure 10 shows bottom-La thickness dependence of Tinv for HfCN gate and EOT for FUSI gate. By comparing the both dependences, we can conclude that Tinv for HfCN gate were reduced by HfCN gate in the case of small amount of La incorporation. This Tinv reduction is presumably due to the oxygen scavenging effect of HfCN and favorable to pMOS in which La can not be used for Tinv scaling.

4. Conclusion

We propose the bottom-La inserted HfSiON gate dielectrics with MOCVD HfCN metal gate electrode. By using the bottom-La process, a robust Vth controllability can be obtained, without serious mobility degradation. The bottom-La process successfully provides drastic reliability improvements in nMOS. MOCVD HfCN metal gate dielectric provides a reduction of Tinv mismatch between nMOS and pMOS. This process will be promising for gate-first fabrication of HK/MG CMOS in 28nm node and beyond.

References

(a) bottom-La
- IFL Formation
- HfSiO Deposition
- Plasma Nitridation
- Post Nitridation Annealing

(b) top-La
- IFL Formation
- HfSiO Deposition
- Plasma Nitridation
- Post Nitridation Annealing
- La Deposition

Fig. 1 Process flows and stack structures of (a) bottom-La inserted HfSiON and (b) La-capped (top-La) HfSiON. In the case of bottom-La, La is directly placed at the dipole formation position.

- $V_{fb}$ shift (V)
- EOT (nm)
- $V_{th}$ shift (V)
- $V_{th}$ (V)
- $N_s$ (cm$^{-2}$)
- $J_{g}$ (gate+) (A/cm$^2$)
- $T_{inv}$ (HfCN gate) (nm)
- $T_{eff}$ (nm)
- $T_{Si}$ (nm)

Fig. 3 $V_{fb}$ dependence on inserted bottom-La thickness. Ni-FUSI gate was used. Robust $V_{fb}$ controllability was achieved.

Fig. 4 EOT dependence on inserted bottom-La thickness. Ni-FUSI gate was used.

Fig. 5 HR-RBS spectrum of bottom-La inserted HfSiON. 0.3nm thick La was deposited before HfSiO$_x$ deposition.

Fig. 6 $J_{g}$ (gate+)-EOT relationship of HfSiON w/ and w/o bottom-La. Ni-FUSI gate was used. ITRS 28nm LOP and LSTP targets are also shown.

Fig. 7 Surface carrier density dependence of (a) effective electron and (b) effective hole mobility in MOCVD-HfCN/HfSiON gate stacks.

Fig. 8 C-V characteristics of HfCN/HfSiON/SiO$_2$ gate stack w/ and w/o bottom-La insertion.

Fig. 9 $V_{fb}$ distributions within 300mm wafer for HfCN/HfSiON w/ and w/o bottom-La insertion.

Fig. 10 La thickness dependence of $T_{inv}$. Turn-around behavior was shown in the case of HfCN gate electrode.

Fig. 11 Surface carrier density dependence of electron effective mobility in HfCN/HfSiON w/ and w/o bottom-La insertion.

Fig. 12 Trade-off relationship between $V_{fb}$ shift and mobility degradation.

Fig. 13 PBTI characteristics of HfCN/HfSiON nMOS w/ or w/o bottom-La insertion. Drastic improvement was obtained by La incorporation.

Fig. 14 TDDB characteristics of HfCN/HfSiON nMOS w/ or w/o bottom-La insertion. Drastic improvement was obtained by La incorporation.