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Influence of Gate Electrode Stress on Channel Stress and Device Performance in Gate-First W/TiN Gate MOSFETs

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Introduction

The stress introduction techniques have been indispensable for high performance CMOSFETs, such as SiGe source/drain for the compressive stress in pMOSFET or stress liner over the top of transistor for the tensile stress in nMOSFET [1, 2]. The control of the channel stress by both selecting the material and controlling process parameter of stress source is required for the manufacturing. Metal/high-k gate stack fabricated with gate-last or gate-first process is also indispensable for avoiding gate depletion and gate leakage current. The metal gate electrode should be considered as a stress source for the channel stress. The gate electrode stress of a gate-last MOSFET with W/TiN gate electrode modulates drain current drivability [3]. In gate-last process, the thermal budget of the post-gate electrode fabrication is suppressed under 500°C. In the gate-first process, the stress of the gate electrode has not been defined due to the higher temperature annealing for formation of the source/drain applied after the gate fabrication.

In this study, the stress of gate electrode and the influence of the gate electrode on the channel stress of a gate-first W/TiN gate MOSFET were investigated with combination of electrical analysis and physical analysis of channel region.

Experimental procedure

nMOSFETs with W/TiN gate were fabricated with a gate-first process (Fig. 1). The tungsten film was deposited by DC sputtering with various thicknesses, PVD-W. The PVD- W films have compressive stress. The compressive stress increased with increasing thickness of the W. The TiN film was deposited by CVD at 10 nm on HfSiON/SiO_2 gate dielectric. The W/TiN/HfSiON/SiO_2 stack was formed into gate electrode with a CVD-SiN hard mask. Spike annealing at 1000°C was performed after source and drain ion implantation. The channel stress was analyzed by combination of a split-HOLZ (High order Laue zone) method and a finite element method [4]. Nano-structure of the MOSEFT and crystallinity of the channel region were analyzed by STEM or TEM.

Results and discussion

Electrical analysis

Maximum transconductance Gm.max is plotted as a function of the W film thickness with gate length Lg of 0.1, 0.4 and 2 μm (Fig. 2). The Gm.max increased with increase of the W film thickness. The Gm.max is plotted as a function of Lg (Fig. 3). It is observed that the Gm.max much changed at Lg ~ 0.4 μm. The sensitivity of the change of Gm.max to the W film thickness is quantified by normalization of Gm.max with the thickness (Fig. 4). A peak is observed in the characteristics of the sensitivity as a function of gate length. Given that the W of the gate electrode has compressive stress after the spike annealing at high-temperature, the increase of the sensitivity at Lg less than ~ 0.4 μm can be explained as performance enhancement by introduction of the tensile stress at the channel. The decrease of the sensitivity at Lg > 0.4 μm can be explained as a relaxation of the channel tensile stress or as an introduction of compressive stress into the channel region based on that the Gm.max is mainly affected by the channel stress..

Channel stress analysis

The cross sectional STEM views of the MOSFETs obtained in the split-HOLZ method revealed the defect introduction into the NiSi edge next to the channel in the case with Lg=0.4 and 2 μm (Fig. 5 (b), (c)). In the case with the Lg=2 μm, dislocations are observed in the channel region (Fig. 5 (c)). TEM analysis indicates that the defect at the NiSi is large dislocations or staking fault with diffraction vector $\mathbf{g} = \bar{4}\bar{4}0$ and formed in the (111) plane (Fig. 6).

The stress analysis with the split-HOLZ method combined with the finite element method applied to the Lg=0.1 μm sample which has no observable defect (Fig. 5(a)). The analysis gave that the W/TiN gate electrode and NiSi had compressive stress of -0.8, -2.4 GPa, respectively. The stress distribution at the channel and the source/drain region was simulated with the stress data of the W and NiSi under condition of no-stress relaxation (Fig. 7). Longer gate length leads to larger tensile stress in channel region due to the gate electrode stress, and leads to larger compressive stress at the NiSi edge due to the stress of the NiSi. If there was no relaxation of the stress in the channel, the sensitivity of the Gm.max should increase with the Lg based on the simulated stress data. However the dislocation at the NiSi edge is presumably introduced by the higher compressive stress building up at the edge in the longer gate length (Fig. 8).Considering the dislocation introduction in the longer Lg, the decrease of the sensitivity at Lg > 0.4 μm, shown in Fig. 4, is explained as a relaxation of the channel tensile stress due to introduction of the dislocations at the edge of the NiSi or in the channel region. It has been also found that the compressive stress built up by the NiSi possibly leads to the degradation of nMOSFET performance in shorter gate length.

Conclusion

The stress analysis by STEM, TEM and a spilt-HOLZ method combined with a finite element method gives practical stress value of the gate electrode of gate-first MOSFET. This study has been revealed that the performance of the gate-first metal/high-k MOSFET can be strongly modulated not only by the gate electrode stress but also by the silicide on the source/drain, and that the silicide formation induced compressive stress resulting in the performance degradation of the nMOSFET.

References

[1] S. Thompson et al., TED 51 (2004) p. 1790.
[2] S. Ito et al., IEDM (2000) p. 247.
[3] T. Matsuki, et al., JJAP (2007) p. 3181.
[4] T. Soeda, Proc. 16th Int. Microscopy Conf., (2006) p. 1021.

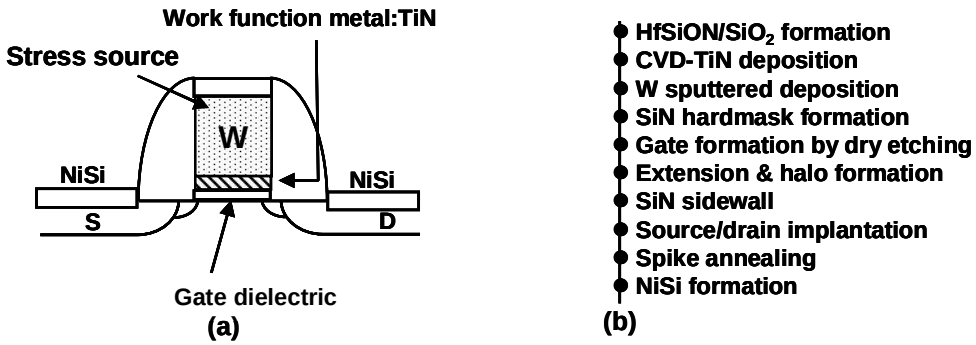


Fig. 1 (a) Schematic view of gate-first MOSFET with W/TiN/HfSiON/SiO_2 gate stack and Ni salicidation, and (b) process flow of gate stack and source/drain formation.

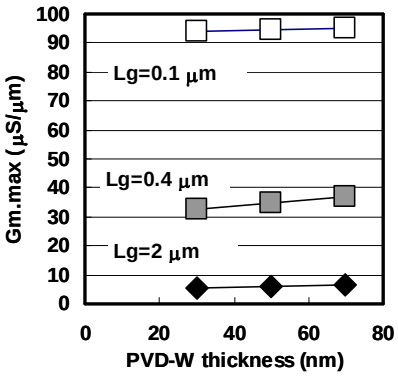


Fig. 2 Maximum transconductance Gm.max as a function of W film thickness.

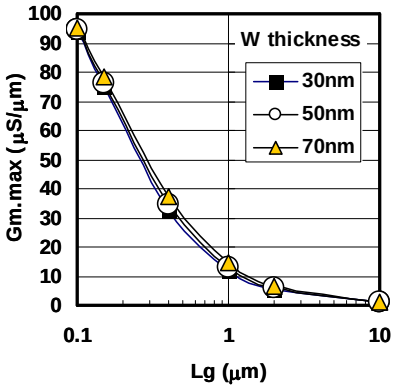


Fig. 3 Gm.max as a function of gate length.

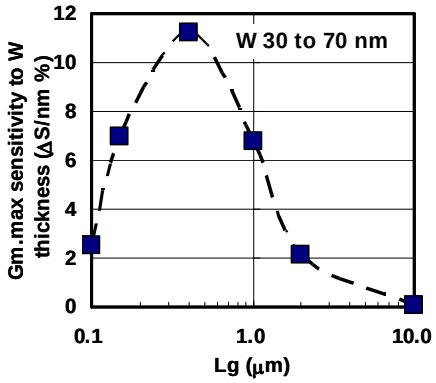


Fig. 4 Gm.max sensitivity to W film thickness as a function of gate length.

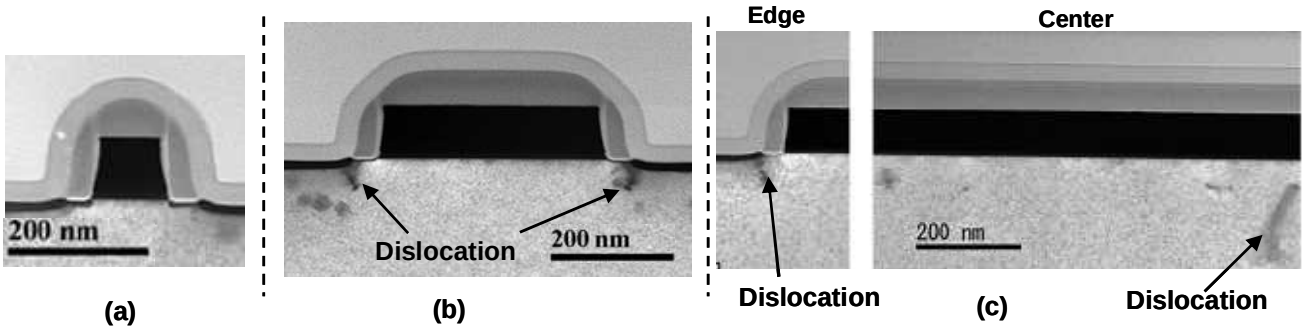


Fig. 5 Cross-sectional STEM views of the W/TiN/HfSiON/SiO_2 gate-first MOSFETs. W= 70 nm. (a) Lg=0.1 μm, (b) Lg=0.4 μm, (c) Lg=2 μm.

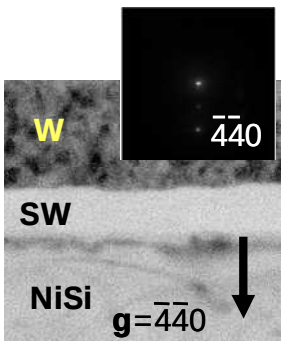
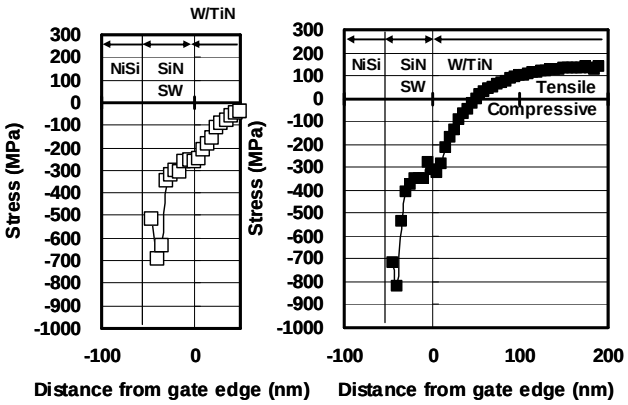


Fig.6 Plan-TEM at the gate edge of the Lg=0.4 μm.. Bright field obtained by the diffraction vector **g** shown in the figure. Inset :The electron diffraction pattern of the bright field view.



(a) Lg=0.1 μm (b) Lg=0.4 μm

Fig.7 Simulated stress distribution in the channel and source/drain region at the depth of 8 nm from the substrate surface. (a) Lg=0.1 μm, (b) Lg=0.4 μm.

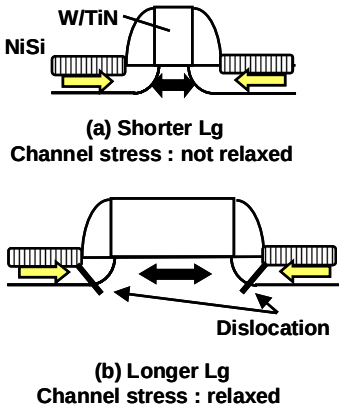


Fig. 8 Schematic model of the channel stress relaxation due to introduction of dislocation at the NiSi edge.