Advanced Low Temperature Raised S/D Epitaxy Using Cyclic and Poly-Selective Techniques

Nicolas Loubet¹, Prasanna Khare¹, Qing Liu¹, Mariko Takayanagi², and Ron Sampson¹

¹STMicroelectronics, Inc.
²Toshiba America Electronic Components, Inc.
Albany Nano-tech., 257 Fuller Road, Albany, NY 12203 USA
Phone: +1-518-292-7220 E-mail: nloub@us.ibm.com

1. Introduction

Raised source/drain (RSD) epitaxy is often considered as a strong solution to resolve CMOS scaling issues such as shallow junction formation and low sheet resistance [1]. This process step is also mandatory for fully-depleted SOI structures in order to enable silicide formation [2]. However, RSD epitaxy integration has some challenges, in particular the simultaneous growth of polysilicon (poly-Si) on top of the transistor gates if no protecting hard-mask is used. This problem can be addressed by employing a protective oxide or nitride hard mask on gates but it often can lead to spacer damage and/or silicidation issues.

In this paper, a new interesting technique will be presented to suppress poly-Si growth without adding any protective hard mask on top of the gates. This technique is based on cyclic epitaxial deposition of silicon and its etch back using HCl gas, a process which is available in any industrial rapid-thermal chemical vapor deposition (RTCVD) reactor. Indeed, the HCl gas is able to remove poly-Si with a great selectivity compared to the monocrystalline phase of silicon (mono-Si) [3]. With optimized process conditions, we can adjust the growth and etch steps in such a way that growth on poly-Si is suppressed, i.e. we effectively get a poly-selective epitaxy (PSE). We will report the activation energies ($E_a$) of both deposition and etch process, using chlorinated chemistries (dichlorosilane (DCS) and hydrides (silane SiH₄)) during the growth steps, with HCl being used as an etching precursor. In particular, the use of silane-based chemistry can be very attractive as deposition occurs at low temperature (T<700°C), unlike chlorine-based chemistries (T>700°C).

Growth rate ratio $\rho=\frac{GR_{PolySi}}{GR_{MonoSi}}$ will be compared and commented for the different deposition precursors as well as the etch selectivity (S), defined as $S=\frac{ER_{PolySi}}{ER_{MonoSi}}$. Finally, the optimized PSE process will be used on CMOS wafers in 32nm technology node, thus demonstrating the capability of this process to suppress parasitic poly-Si growth on top of the gates.

2. Experimental

All experiments were carried out in an Applied Materials 300mm wafer industrial RTCVD (Rapid Thermal CVD) reactor. Conventional blanket (100)-wafers were used to determine the growth and etch rates of both mono-Si and poly-Si. For mono-Si, $GR_{MonoSi}$ and $ER_{MonoSi}$ were measured with ellipsometry using a thin SiGe marker layer below the silicon (Fig.1a). Concerning poly-Si, growth on thermal oxide ($GR_{PolySi/SiO2}$) was first determined using the same chemistry as mono-Si growth and thus obtained poly-Si wafers were reused after 1min pre-bake at 850°C to obtain $GR_{PolySi/PolySi}$ and $ER_{PolySi}$ (Fig.1b). Patterned wafers containing both poly-Si and mono-Si areas were employed to optimize the PSE process on device lots.

In both cases, experiments were performed with the same moderate partial pressure $P_{DCS}=P_{SiH₄}=0.16$Torr, considering 50nm silicon growth but using an appropriate range of temperatures depending on the used deposition chemistry. In order to compare similar growth rates, we considered the 675°C-750°C temperature range for deposition with DCS and 575°C-650°C for SiH₄. In a similar way, etching of silicon was realized employing the simple HCl/H₂ gas mixture with $P_{HCl}=12$Torr and 675°C< T<750°C for DCS-grown films versus $P_{HCl}=370$Torr and 625°C< T<700°C for SiH₄-grown films. Indeed, we demon-

3. Results

We report in Figure 2 the Arrhenius plots of the growth and etch of mono and poly-Si for chlorinated (Cl-based) chemistries and hydrides (H-based), using DCS/HCl (Fig.2a) and SiH₄/HCl (Fig.2b), respectively.

![Fig. 1: Experiments for GR and ER extraction of mono/poly-Si growth and etch rates](image)

![Fig. 2: Arrhenius plots of the growth and etch rates of silicon using DCS (a) and SiH₄ (b), HCl is employed as etching precursor](image)
strated in previous studies [4] that increasing the HCl partial pressure gave access to lower etch temperatures. From the Arrhenius plots slopes, the activation energies $E_a$ of both growth and etch processes were extracted. These values are reported in Table I.

Table I : Extracted activation energies

<table>
<thead>
<tr>
<th>Cl-based DCS/HCl</th>
<th>H-based SiH$_4$/HCl</th>
</tr>
</thead>
<tbody>
<tr>
<td>$GR_{MonoSi}$</td>
<td>$60$</td>
</tr>
<tr>
<td>$PolySi$/$PolySi$</td>
<td>$58$</td>
</tr>
<tr>
<td>$ER_{MonoSi}$</td>
<td>$65$</td>
</tr>
<tr>
<td>$PolySi$/$PolySi$</td>
<td>$65$</td>
</tr>
</tbody>
</table>

$GR$ and $ER$ of Poly/Mono-Si using DCS/HCl

It is interesting to note that the growth of silicon using DCS is totally selective to SiO$_2$, i.e. $GR_{PolySi}/SiO_2=0$ in the considered temperature range (675°C-750°C). The $E_a$ values associated with both mono/poly-Si growth are very close, in the range 58-60 kcal/mol and consequently $\rho$ is constant at low temperature (T<750°C) with $\rho$=1.1. The etch of mono-Si and poly-Si using $P_{HCl}=127$Torr exhibits slightly higher activation energies, about 65 kcal/mol, and etch selectivity is constant as a function of temperature. We found $S=9\pm 1$ over the entire temperature range.

$GR$ and $ER$ of Poly/Mono-Si using SiH$_4$/HCl

If we consider the case of hydrogenated chemistries (growth with SiH$_4$ only), it is more complex as the deposition is not selective to oxide if no Cl is added in the gas phase. Therefore, silicon growth occurs even on simple SiO$_2$ layers. In this case, low $E_a$ values are obtained, 49 kcal/mol for the epitaxy of mono-Si, 42 kcal/mol for poly-Si growth on SiO$_2$ and finally 46 kcal/mol for poly-Si on poly-Si. The growth rate ratio $\rho$ was found constant in the range 600°C-650°C with $\rho$=1.37 but increases towards the lowest temperatures: $\rho$=1.6 at 757°C. Concerning etching of silicon, a higher HCI partial pressure was used in this case ($P_{HCl}=370Torr$) and a slightly lower etch selectivity and $E_a$ extracted. We found $S=7.5\pm 1.5$ and for mono and poly-Si, $E_a=52-53$ kcal/mol at high $P_{HCl}$.

Note that in any case, $GR_{PolySi/\text{SiO}_2}$ is always higher than $GR_{Polys\text{Si}/PolySI}$. It is quite an interesting result and consequently proves that even if we obtain $GR_{PolySi/\text{SiO}_2}=0$ on recrystallized poly-Si it will be difficult to build an efficient PSE process using SiH$_4$ with the presence of both SiO$_2$ (STI) and poly-Si on wafer, as the deposition will still occur on SiO$_2$.

PSE process on patterned and CMOS devices wafers

We extracted $\rho$ and $S$ parameters over a wide range of temperatures for silicon growth and etch using DCS/HCl. To optimize this process, patterned wafers containing only poly-Si and mono-Si were used and the growth and etch step times were adjusted in order to obtain poly-Si growth close to zero. We used 750°C for both deposition and etch of silicon. Figure 3 reports cumulative deposition obtained after PSE tuning resulting in deposition of 30nm mono-Si (Fig.3a) while no growth of poly-Si (Fig.3b).

3. Conclusions

We demonstrated the efficiency of PSE technique, based on cyclic growth and etch steps, to suppress poly-Si growth on top of the gates in RSD epitaxy integration. All poly/mono-Si growth and etch ratios were extracted in chlorinated (DCS) and hydride (SiH$_4$) chemistries as well as the activation energies. We showed that it is not possible to obtain a PSE process with SiH$_4$ (hydride chemistries), with a good selectivity against the dielectrics, an oxide or nitride hard mask on top of the gates being mandatory. However, PSE with DCS gas can entirely suppress poly-Si growth and enables the integration of RSD epitaxy in very dense devices for the 32nm node and beyond. Finally, this technique can be extended to all chlorinated deposition precursors and to the epitaxy of alloys such as SiGeC, as etching of polycrystalline phases of these materials is always faster than monocrystalline phases.

Acknowledgements

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

References