

First LSI Applicable Thin SOI Films Formed by Lateral Solid Phase Epitaxy

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1. Introduction

Lateral solid phase epitaxy (L-SPE) has been researched for making partial SOI substrates for a long time [1-6]. However, only few works have reported on the fabrication of SOI MOS-FETs [3,4]. Since Si crystal made by L-SPE has to be annealed from amorphous phase at low temperature in order to obtain a wide SOI area, many defects are inevitably remained in Si crystal.

We fabricated thin SOI film by L-SPE with LSI applicable quality for the first time by means of thinning-oxidation and striped oxidation technique of the SOI layer, where the stripe was across the lines of the seed for L-SPE. Quality of SOI films was confirmed by photoluminescence. Operation of NAND cell revealed the LSI of the SOI film formed by L-SPE.

2. Experiment

Fabrication process of thin SOI film is shown in Fig. 1. SiO₂ layer was removed partially for the seed formation. The pattern was narrow lines of Si exposed area (seed area) and wide SiO₂ area (SOI area). The lines for seed area were parallel to <100> direction. Then amorphous Si (a-Si) of 300nm was deposited by LPCVD with the *in-situ* pre-cleaning step for native oxide removal. The a-Si layer is annealed at 550 °C for L-SPE for 24 hours. The crystallized layer was then thinned by plain oxidation or RIE.

After the oxide layer was removed, striped oxidation was performed on the SOI film. The stripes were across the seed lines. L-SPE SOI layer was analyzed by transmission electron microscope (TEM) and Photo luminescence (PL). NAND cell with depletion-type cell transistor was fabricated on L-SPE films.

3. Results and Discussion

One of the well-known issues for fabricating SOI by L-SPE is to make a sufficiently wide SOI area. These issues were overcome by the selection of the direction of L-SPE [5] and the thickness of the film during L-SPE [6].

Figure 2 shows the crystal direction dependence of L-SPE. Figure 2(a) shows the results of 45° notch wafer, where L-SPE growth direction was <100>, and Fig. 2(b) was 0° notch wafer, where L-SPE growth direction was <110>. In the case of L-SPE growth for <110>, there were many twin defects in the crystal (Fig.2 (b)). There were few defects in the L-SPE layer to <100> direction, and L-SPE grows longer than to <110> direction. Growth front to <110> direction changes easily to {111} facet, thus twin boundaries are easily made and L-SPE growth speed is slow.

Thickness dependence of the a-Si layer on the length of the L-SPE region is shown in Fig. 3. By setting the thickness of a-Si

300nm, SOI layer having the length of 2.5μm from the seed, which means the width of 5.0 μm between the neighboring seeds, can be formed.

Thickening the initial a-Si layer has another advantage on the fabrication of SOI by L-SPE. Flat surface is difficult to be obtained because of the step at the seed region. The seeds width was studied in Fig. 4. The narrow seeds width enables to make high proportion of SOI area and to fill dimple upper of seeds while deposition. Fig. 4(a) shows dependence of the depth of dimple above seeds on the seed-width when a-Si deposited 300nm. Fig. 4(b) shows TEM image around seed area after L-SPE anneal.

In the case 300nm-thick a-Si, the depth of dimple decreased by the narrowing of seeds width (Fig. 4(a)). The thickness of a-Si layer decreased the depth of dimple. When the a-Si layer thickness was thin, the narrow seeds width needed. Fig. 4(b) shows a TEM image of SOI made by L-SPE with seed width 50nm. The seeds width 50nm was enough to work as epitaxial seeds and single crystal was grown. The dimple above seeds was nearly flat at 150nm a-Si thickness. Ideally the narrow seeds width is better. However, it is difficult to make narrow seeds having clean interface and the epitaxial growth might be suppressed. Thus, seed with the width of 50nm was used for L-SPE SOI formation.

Oxidation of SOI layer is effectively used to improve the quality. Both RIE and oxidation can be used for thinning the SOI, which is essential for this L-SPE process using thick a-Si. Figure 5 shows plane TEM images researching removed defect in SOI layer. Figure 5 (a) shows after L-SPE, and Fig. 5(b) shows after oxidized with H₂O atmosphere at 950 °C. Right after L-SPE, there were a lot of defects in the SOI layer and subgrainboundary at the center of the seeds (Fig.5 (a)). After the oxidation step, most of small defects were removed as shown in Fig. 5 (b). It was revealed from PL spectra for the samples before and after oxidation that oxidation induces the reduction of defects (Fig.6). The intensity of FE^{TO}-c-Si, which indicates good crystallinity of the films. However, line shape defects, such as subgrainboundaries at the center of the seeds, were remained as shown in Fig. 5(b). D lines in PL spectra in Fig. 6 also indicate existence of dislocations.

Additional striped oxidation has drastic influence in eliminating the defects. TEM images of the sample with striped oxidation in Fig. 7 shows the effect of striped oxidation, where striped pattern was formed across the seed and the SOI was oxidized as shown in Fig. 1. Oxidation temperature was 800 °C. Most of the defects in the L-SPE SOI layer were disappeared after the striped oxidation. Subgrainboundary at the center of the neighboring seeds, which could not be avoided in the formation of SOI by L-SPE, was not observed.

Defects in the L-SPE layer might originate from the low density of a-Si. Thus, the defect is the cluster of vacancies. Oxidation process supplies interstitials to the film and the defects could be vanished due to the recombination of interstitials and vacancy-rich defects. From the standpoint of supplying interstitials and moving the defect to the interface between SOI films and SiO₂, stripe oxidation technique is the most appropriate process.

Figure 8 shows one of the examples that NAND cells fabricated on the SOI by means of L-SPE method. Figure 8 (a) shows TEM image of NAND cells on SOI. The SOI thickness of 30nm was achieved. The NAND cell on SOI works different from the one on Si substrate. This works depleting SOI channel region, and turning off channel current. It is called **Depletion-type cell-Transistor on a Partial SOI-substrate (D-ToPS)** [7]. Figure 8(b) shows the I-V curve of NAND cells. Operation of NAND cells on the SOI by L-SPE method was confirmed.

3. Conclusions

We studied fabricating the thin and high quality SOI layer by L-SPE method. By deposition a-Si film of 300nm with the <100> seed, the width of which was 50nm, SOI layer of 5.0 μm width with flat surface was obtained. The oxidation step revealed to be effective to reduce the defects. By applying the

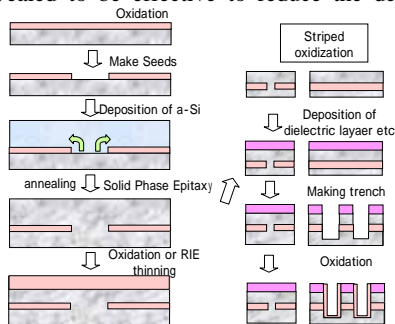


Fig. 1 Fabrication of SOI layer. Direction of striped oxidation was across the seed lines. Striped oxidation can serve as isolation.

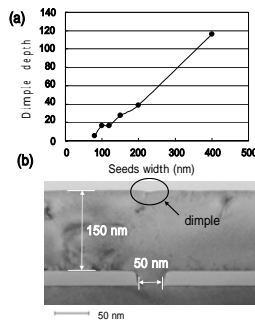


Fig. 4 (a) Dimple depth depends on seeds-width with a-Si 300nm, (b) TEM image of seed width 50nm, after L-SPE anneal.

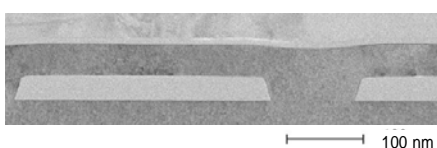


Fig. 7 TEM image of SOI between the neighboring seeds after striped oxidation.

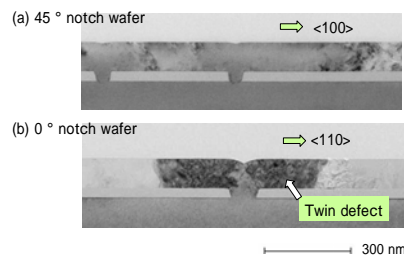


Fig. 2 Lateral Solid Phase Epitaxy Crystal direction dependence.

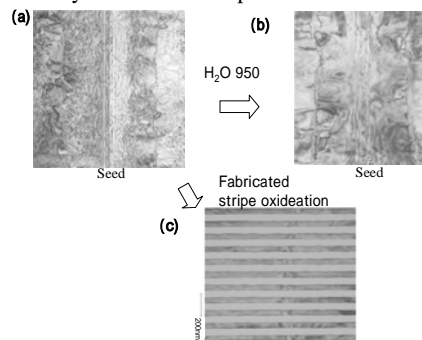


Fig. 5 Plane TEM images of L-SPE SOI before and after oxidation.

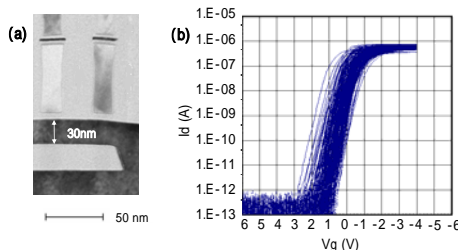


Fig. 8 (a) TEM image of NAND cell on SOI and (b) I-V characteristics of NAND cells.

striped oxidation, most of the defects including the subgrainboundary at the center of the neighboring seeds were removed from SOI layer.

We demonstrated NAND cells on SOI by L-SPE and confirmed the function of NAND cells and applicability to LSI. The proposed technique to improve the quality of L-SPE SOI layer could be useful for various MOSFET applications on with local SOI structure.

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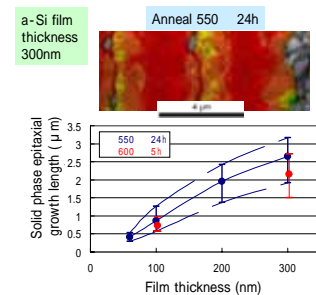


Fig. 3 Lateral solid phase epitaxial growth, film thickness dependence.

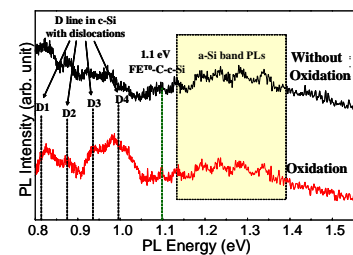


Fig. 6 PL spectra for samples without oxidation and with oxidation. FE^{TO}-c-Si peak clearly indicates good crystallinity of L-SPE film by oxidation condition.