High Electron Mobility Ge n-Channel MOSFETs with GeO2 grown by High Pressure Oxidation

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1. Introduction

Germanium (Ge) MOSFETs have recently attracted much attention in terms of high electron and hole mobility in bulk Ge, and its low processing temperature is compatible with high-k dielectrics. Up to now, however, poor electrical characteristics of Ge n-channel MOSFETs have been reported [1-4], while Ge p-MOSFETs show the hole mobility much higher than Si ones [5]. Many research groups have failed to solve the n-MOSFETs problems because it is hard to achieve both high quality Ge/dielectric interface and high activation of n-type impurities. We reported that high-pressure oxidation (HPO) of Ge was very effective to suppress the GeO desorption even at 600 °C, and demonstrated a significant improvement in electrical properties of Ge/GeO2 interface [6]. In this paper, the highest electron mobility in Ge n-MOSFETs fabricated to date is reported.

2. Device Fabrication

The Ge nMOSFETs were fabricated on (100) oriented p-type Ge substrates with a resistivity of 2 ~ 3 Ωcm. After chemically cleaning the Ge substrates followed by diluted HF solution, 50nm-Y2O3 and 500nm-spin on glass (SOG) were deposited for the purpose of a spacer and field oxide, respectively, as shown in Fig. 1(a). Several channel lengths (W/L = 90 μm/100~500 μm) were defined, and phosphorus (1 x 1015 /cm2 dose) was implanted with 100 KeV to make source/drain junction, as shown in Fig. 1(b) and Fig. 1(c). The thermal oxidation of Ge and the activation of phosphorus-doped Ge junction were performed simultaneously by HPO, where HPO was carried out at 550°C for 10 min with 70-atm O2. Then, a low temperature oxygen annealing (LOA) was performed at 400°C for 10 min with 70-atm O2. Finally, Al was deposited by vacuum evaporation and gate electrode was defined. Fig. 1(d) shows the schematic structure of the fabricated Ge n-MOSFET. Note that Y2O3 spacer was used to protect GeO2 from the wet process and air exposure.

3. Results and Discussion

Fig. 2(a) shows bi-directional capacitance-voltage (C-V) characteristics of the fabricated Al/GeO2/Ge n-MOSFETs. The GeO2 thickness in device was 8.5 nm estimated from the saturated capacitance of C-V characteristics, where the dielectric constant of HPO-GeO2 was used [7]. A very small hysteresis and frequency dispersion indicate that the superiority of Ge/GeO2 interface properties is well kept even after MOSFETs fabrication. Fig. 2(b) shows current-voltage (I-V) characteristics in n+/p junction at source/drain (S/D) after Ge nMOSFETs fabrication. It shows good rectifying diode characteristics with the reasonable reverse leakage current, and the on-off current ratio of 6.2 x 104 is achieved. From the results of n+/p junction and MIS characteristics as shown in Fig. 2, it is concluded that HPO is really feasible for device fabrication process. Fig. 3 shows the energy distribution of the interface states density (Dit) estimated by the conductance method at low temperatures (100K to 200K). It is shown that the minimum value of Dit in Ge/GeO2 MISCAPs with HPO is as low as 2x1011 eV-1cm-2, and it is further reduced by LOA down to below 1011 eV-1cm-2.

The well-behaved IS-VG and ID-VD characteristics of the fabricated Ge nMOSFETs with channel width/length = 90 μm/300 μm are shown in Fig. 4. The good Ion/Ioff current ratio (104) at VD = 1V and the subthreshold slope of 130 mV/dec are achieved (The calculated D factor from the subthreshold slope is about 3x1012 eV-1cm-2). Fig. 5 shows the extracted electron mobility as a function of inversion carrier density (N_i), where N_i was estimated by qN_i = C_V(VGS-Vth). By using several channel lengths of nMOSFETs, the parasitic resistance (R_MOS) = 3.5 KΩ was taken into consideration to estimate the intrinsic mobility. The peak electron mobility is above 700 cm2/Vs at room temperature. This is the highest electron mobility to date in Ge MOSFETs and quite comparable to Si universal mobility. The low D factor may be a predominant origin for high mobility. The extracted electron mobility, however, is still lower than expected, possibly due to coulomb scattering from the remaining fixed charges and/or relatively larger surface roughness at the interface [8]. The surface roughness was measured by AFM, and it reveals that surface roughness of Ge is about 3 times larger than that of Si. Thus, by improving both them, the electron mobility should be further improved.

4. Conclusion

High performance Ge n-channel MOSFETs with
Al/GeO₂/Ge gate stack have been successfully fabricated, where GeO₂ was grown by HPO and LOA and both superior Ge/GeO₂ interface properties and good S/D junction characteristics were achieved simultaneously. Ge n-MOSFETs exhibited the peak electron mobility above 700 cm²/Vs at room temperature, which is the highest to date in Ge MOSFETs. It is inferred that significant improvement of electron mobility is thanks to the reduction of the coulomb scattering centers through HPO followed by LOA.

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References


Fig. 1. Schematic process flow of Ge n-MOSFETs. (a) Active area definition by SOG etching, (b) phosphorus (1 x 10¹⁵/cm²) implantation with 100 KeV for S/D junction, (c) Y₂O₃ etching for spacer formation, and (d) Impurity activation and thermal oxidation of Ge by HPO and LOA.

Fig. 2. (a) Bi-directional C-V characteristics of the fabricated Al/GeO₂/Ge gate stack n-MOSFETs, where GeO₂ was grown by HPO and LOA. (b) I-V junction characteristics of n+/p junction at S/D of n-MOSFETs.

Fig. 3. Energy distribution of Dit estimated by the conductance method at 100K to 200K.

Fig. 4. (a) Transfer characteristics (Iₓ-Vₓ) of n-MOSFETs. The Ion/Ioff current ratio at Vₓ = 1V is about ~10⁴, and the subthreshold slope of 130mV/dec is achieved. (b) Well-behaved output characteristics (Iₓ-Vₓ) of n-MOSFETs. Here, L/W = 300 μm /90 μm.

Fig. 5. Extracted electron mobility as a function of inversion carrier density. The peak electron mobility is above 700 cm²/Vs at room temperature. This is the highest electron mobility to date in Ge MOSFETs and quite comparable to the Si universal mobility.