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Effects of MIS Interfacial Layers on Interface Trap Density near Conduction Band Edge in Ge MIS Structures

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1. Introduction

MISFETs with Ge channels have attracted much attention as next generation CMOS devices because of its high bulk electron and hole mobilities. In fact, the high performances of Ge p-channel MISFETs with Si or GeO_2 interfacial layers (IL) have already been demonstrated [1-4]. On the other hand, Ge n-channel MISFETs with Si or GeO_2 IL have not realized the performance expected from the bulk electron mobility [5, 6]. Martens *et al.* have reported that this insufficient mobility of the Ge nMISFETs with Si IL is attributable to a large amount of interface traps near the conduction band edge (CBE) [7]. In addition, they have also reported for $HfO_2/SiO_2/Si/Ge$ gate stacks that these interface traps are the acceptor type [8]. However, the validity and the accuracy of these analyses have not been examined yet, because of the complicated behaviors of defects near Ge MIS interfaces. In addition, the effects of Ge MIS ILs on interface trap density (D_{it}) near CBE have not been fully studied yet.

In this study, we systematically study the interface properties of the Ge MIS capacitors with Si or GeO_2 IL by employing two different evaluation method of D_{it} in order to examine the accuracy of measured D_{it} values. It is found that the Si ILs induce a large amount of the interface traps near CBE, while GeO_2 IL is effective to reduce the interface traps near CBE. Also, the interface traps near CBE at the MIS interfaces with both the ILs are identified to have the acceptor nature.

2. Experimental

The fabrication process flow of the capacitors and the resulting gate stack structures are shown in Fig. 1(a) and 1(b), respectively. In the case of capacitors with Si IL, n-type Ge(001) wafers were annealed in H_2 ambient for surface cleaning after the device isolation. Subsequently, Si layers were epitaxially grown on the Ge surfaces by introducing SiH_4 into the H_2 ambient. Next, SiO_2 or HfO_2 layers as gate insulator films were deposited. As for capacitors with GeO_2 IL, Ge wafer were annealed at 420°C in O_2 ambient without H_2 cleaning and the Si epitaxy. Next, SiO_2 layers as a gate insulator films were deposited. Successively, TaN and NiSi gate electrode were formed. C-V and Conductance versus Frequency measurements were carried out at various temperatures.

3. Results and Discussion

Fig. 2(a) and 2(b) show the TEM images of the Si IL capacitor with a Si IL (7 mono layer (ML))/HfO_2 gate stack structure and the GeO_2 IL capacitor, respectively. The epitaxial Si IL and the GeO_2 IL are clearly observed at the insulator/Ge interfaces. Fig. 3 shows the C-V curves of a Si IL capacitor with a Si IL (7ML)/SiO_2 gate stack structure, measured for various frequencies at 300K. The frequency dispersion in the range from 0.5 to 1 V is hardly observed at 300K, while the large dispersion is clearly observed at 180K as shown in Fig. 4. Similar dispersion is observed in the other Si IL capacitors, as also reported in the transistors with $HfO_2/SiO_2/Si/Ge$ stacks [7]. Furthermore, the large flatband voltage (V_{FB}) shifts toward the positive gate bias are observed with decreasing temperature as shown in Fig. 5. Fig. 6 shows the C-V curves of a GeO_2 IL capacitor measured at 180K. The large frequency dispersion is not observed even at low temperatures. Nevertheless, the small but systematic V_{FB} shifts associated with reducing temperature are observed in Fig. 7. The relationships between V_{FB} and temperatures for the Si IL capacitors and the GeO_2 IL capacitors are shown in Fig. 8. The solid line indicates the temperature dependence of E_F-E_i, where E_F and E_i are bulk Fermi level and intrinsic Fermi level of Ge, respectively. In both type of the ILs, V_{FB} is found to shift toward the positive bias direction with decreasing temperature. The values of the shift are much larger than the values expected form the change in E_F-E_i, indicating that a large amount of interface traps exist near CBE and that the interface traps are negatively charged by capturing electrons.

The energy distribution of D_{it} can be accurately evaluated from this temperature dependence of V_{FB}. This is called the Gray-Brown (GB) method [9], where the shift in the band bending associated with the change in E_F-E_i due to the difference in temperature can provide the information of interface charges. For this purpose, V_{FB} needs to be accurately determined without any influence of capacitance associated with the interface traps (C_{it}). Fig. 9 shows the capacitances measured at 80K and 180K around V_{FB} as a function of frequency for the Si (4ML) and GeO_2 IL capacitors. The frequency dependence around 1 MHz is hardly observed, indicating that C_{it} is negligible small around 1MHz at these temperatures and, thus, V_{FB} can be accurately determined. Fig. 10 compares the energy distributions of evaluated from the GB method and the conductance method for the Si IL (4ML) capacitor with the SiO_2 gate insulator and the GeO_2 IL capacitor. A good agreement in D_{it} between the two methods is obtained, indicating the high accuracy of the present D_{it} evaluation. Furthermore, the positive V_{FB} shifts associated with the increase in E_F, seen in Fig.8, means that the almost interface traps distributed near CBE have the acceptor nature. Similar results have been reported for $HfO_2/SiO_2/Si/Ge$ gate stacks through the analyses of the threshold voltage shifts of the n- and p-MISFETs with different Si IL thicknesses [8]. However, this method cannot be sufficiently accurate because of the influence of the variation in oxide fixed charges [10]. In contrast, the present method is much more reliable, because the influence of fixed charges is not included in this method.

Fig. 11 shows the energy distributions of D_{it} for all the investigated capacitors. D_{it} of the Si IL capacitors with HfO_2 gate insulators amounts to around 10^{14} $cm^{-2}eV^{-1}$, which is slightly larger than that of the Si IL capacitors with SiO_2 gate insulators. The large frequency dispersion seen in Fig. 4 and the large V_{FB} shifts seen in Fig. 5 are attributed to a large amount of the interface traps near CBE. On the other hand, D_{it} of the GeO_2 IL capacitors is lower by almost one order of magnitude than that of the Si IL capacitors. This means that ILs have a strong influence on D_{it} near CBE and GeO_2 IL is quite effective in reducing D_{it} near CBE.

4. Conclusions

The GB and the conductance methods have revealed that the Ge MIS capacitors with Si IL have a large amount of the interface traps near CBE. It has been found that the GeO_2 IL is effective to reduce the interface traps near CBE, suggesting the MIS interfaces including GeO_2 IL is promising for high performance Ge nMISFETs. Furthermore, the interface traps of the Si and GeO_2 IL capacitors near CBE were identified to have the acceptor nature.

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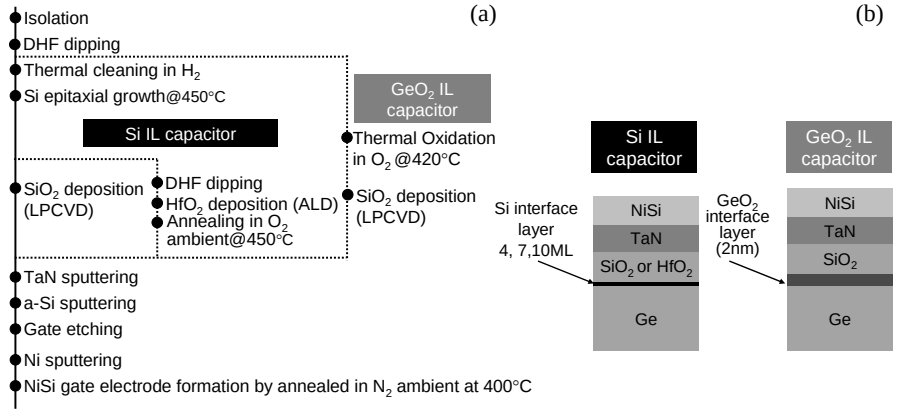

Fig. 1 (a) Fabrication process flow of the capacitors and (b) the gate stack structures of the capacitors with Si IL and GeO_2 IL.

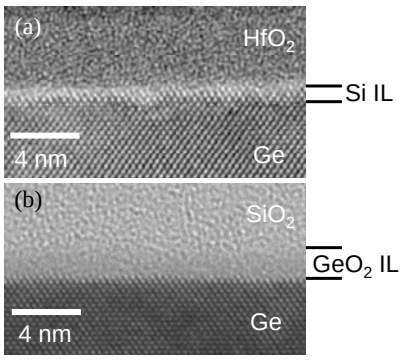

Fig. 2: TEM images of (a) Si IL capacitor with a Si IL(7ML)/HfO_2 gate stack structure and (b) GeO_2 IL capacitor.

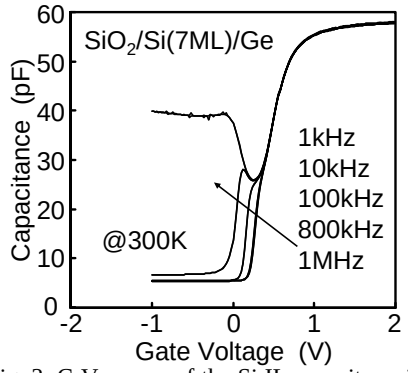

Fig. 3: C-V curves of the Si IL capacitor with a Si IL(7ML)/SiO_2 gate stack structure. C-V curves were measured for various frequencies at 300K.

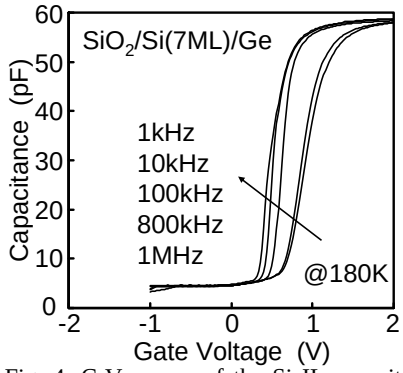

Fig. 4: C-V curves of the Si IL capacitor with a Si IL(7ML)/SiO_2 gate stack structure. C-V curves were measured for various frequencies at 180K.

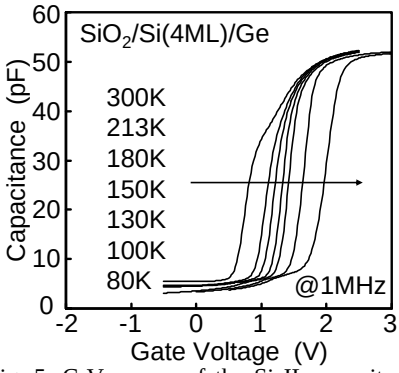

Fig. 5: C-V curves of the Si IL capacitor with a Si IL(4ML)/SiO_2 gate stack structure. C-V curves were measured at various temperatures.

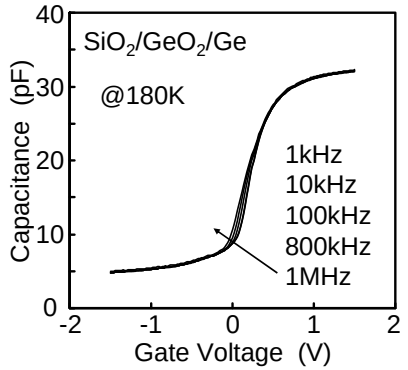

Fig. 6: C-V curves of the GeO_2 IL capacitor measured for various frequencies at 180K.

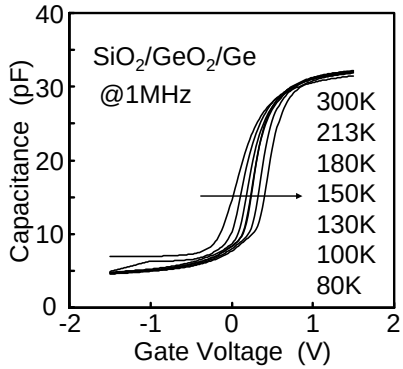

Fig. 7: C-V curves of the GeO_2 IL capacitor measured at various temperatures.

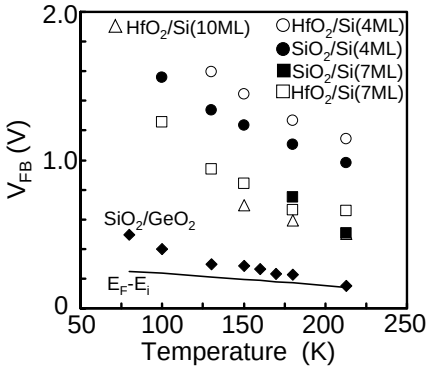

Fig. 8: V_{FB} of the fabricated capacitors as a function of temperatures.

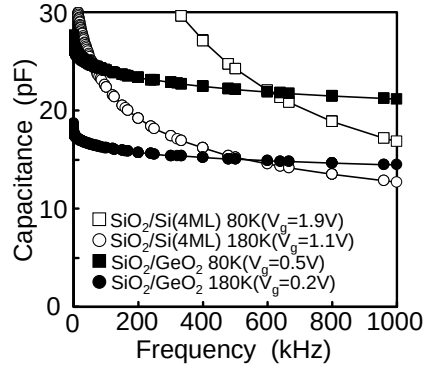

Fig. 9: Capacitances around flatband conditions as a function of frequency. V_g means the gate bias voltage.

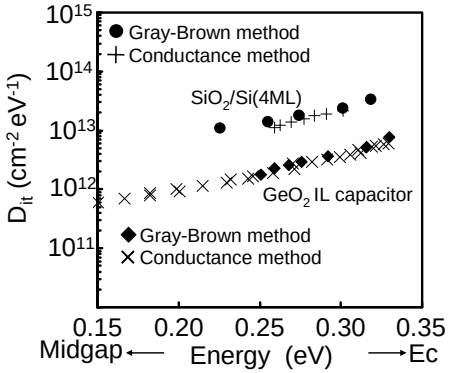

Fig. 10: Comparison of energy distributions of D_{it} evaluated from the Gray-Brown and the conductance methods for the Si IL capacitor and the GeO_2 IL capacitor

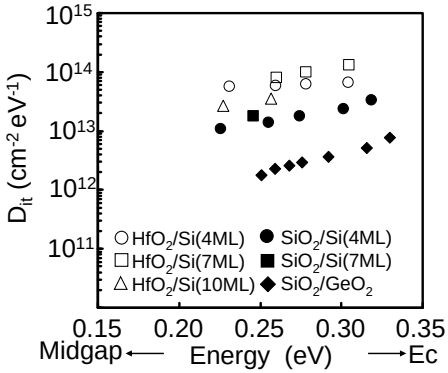

Fig. 11: Energy distribution of D_{it} evaluated from the Gray-Brown method near the conduction band edge.