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Process Condition Dependence of Random V_T Variability in NFETs and PFETs

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1. Abstract

Origins of random V_T variability difference between NFETs and PFETs are investigated. Neither gate structure nor channel stress condition influence the V_T variability. On the other hand, process conditions those affect channel dopant randomness and profile, like channel counter dope and halo carbon co-implantation affect V_T variability. These results support our previous result that V_T variability difference between NFETs and PFETs is dominated by the channel dopant characteristics.

2. Introduction

Random V_T variability is one of barriers which should be overcome to shrink LSI devices. Firstly, the origins of V_T variability should be revealed to control V_T variability.

Pelgrom plot [1] is popular way to evaluate V_T variability. Since V_T variability depends on T_{INV} and N_{SUB}, V_T variability index A_{VT} varies with T_{INV} and N_{SUB} (Fig. 1) [2]. Therefore, it is difficult to compare V_T variability of MOSFETs with different process conditions with Pelgrom plot. Takeuchi plot [3] [4] enables to normalize V_T variability of MOSFETs with different T_{INV} and N_{SUB}. V_T variability index B_{VT} is constant for different T_{INV} and N_{SUB} (Fig. 2) [2].

According to our previous studies [4] [5], PFETs' V_T variability is almost explained by the random channel dopant fluctuation (RDF) with uniform channel profile. On the other hand, NFETs' V_T variability is larger than that of uniform profile RDF model. The enhancement of NFETs V_T variability is can be explained by the enhancement of RDF effect by channel profile nonuniformity [6].

In this study, possibility of other origins and effect of channel dopant (Fig. 3) are investigated by evaluating process dependence of V_T variability with Takeuchi plot.

3. Results and Discussions

Effect of gate electrode

Generally, it is well known that the grain size is different in P-doped and B-doped poly-Si (Fig.4). The effect of gate electrode on NFET and PFET V_T fluctuation difference is investigated by comparing N^+-gate NFET, N^+-gate PFET and P^+-gate PFET electrical characteristics.

The C-V characteristics are shown in Fig.5. The V_{FB} of N^+-gate PFET is shifted by -1.05V from V_{FB} of P^+-gate PFET. This shift indicates that N^+-gate P^+-PFET is properly fabricated. Takeuchi plots N^+-gate NFET, N^+-gate PFET and P^+-gate PFET are shown in Fig.6. B_{VT} of N^+-gate PFET is close to that of P^+-gate PFET and much smaller than that of N^+-gate NFET. This result indicates that N^+-gate makes no contribution to NFET V_T variability enhancement.

Effect of Channel Stress

The stress liner technique is used to enhance carrier mobility. Figure 7 shows the cross sectional TEM image of MOSFET. The stress liner is deposited after the MOSFET structure formation. To evaluate the effect of channel stress on V_T variability, the stress liner condition is varied from compressive stress to tensile stress.

Figure 8 shows the I_{ds}-V_{gs} characteristics of NFET and PFET with variety of the stress liner conditions. The drain current of NFET and PFET are enhanced by the tensile stress and compressive stress liners respectively. This result indicates the stress liner properly works.

Figure 9 compares the B_{VT} of each stress liner condition. Although drain current is modulated by the stress liner condition, B_{VT} is hardly changed by the stress liner condition. From this result, channel stress does not affect V_T variability.

Effect of Counter Dope in Channel

As one of processes which modulate the randomness of channel dopant, effect of counter dope on V_T variability is evaluated. Figure 10 shows A_{VT} and B_{VT} with counter dope. A_{VT} increases as counter dope concentration increases though channel dopant concentrations are same in all counter dope conditions.

This is because that randomness of total dopant atoms increases as the number of channel dopant atoms increases. Compared to A_{VT}, difference of B_{VT} is enhanced because V_T variability increases, even though V_T turns down by the counter dope.

Effect of Halo Carbon Co-Implantation

The halo carbon co-implantation process is known as a method to reduce V_T variability [7]. The halo carbon co-implantation is thought to suppress V_T variability by suppressing boron TED which generates depth and lateral direction channel profile nonuniformity.

Figure 11 shows B_{VT} of various kinds of the halo carbon co-implantation conditions. B_{VT} decreases with the halo carbon co-implantation conditions.

7. Summary

The effect of poly-Si gate electrode and the channel stress do not affect V_T variability. On the other hand, process conditions which affects randomness and profile of channel dopants like the counter dope and the halo carbon co-implantation, affect V_T variability.

These results support our previous result that NFETs V_T variability enhancement is dominated by the channel dopant characteristics [6].

Acknowledgements

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References [1] M. J. M. Pelgrom et al., IEEE Journal of SSC 24, pp.1433-1440, 1989. [2] T. Tsunomura *et. al.*, SSDM, pp.860-861, 2008. [3] K. Takeuchi, SNW Abst., pp.7-8, 2007. [4] K. Takeuchi *et al.*, IEDM tech dig., pp.467-470, 2007. [5] T. Tsunomura *et al.*, VLSI tech, pp.156-157, 2008. [6] T. Tsunomura *et al.*, VLSI tech, pp.110-111, 2009. [7] S. Ekbote *et al.*, VLSI tech., pp.160-161, 2008.

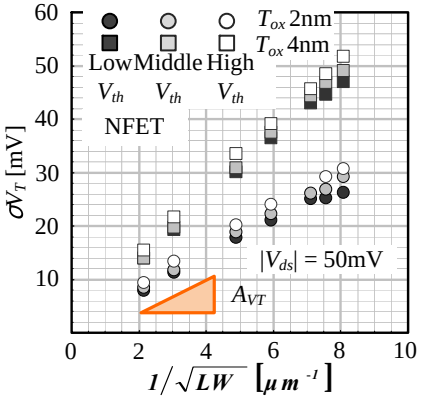

Fig.1 Pelgrom plot of MOSFETs for various kind of T_{INV} and N_{SUB}. (Reprinted from [2])

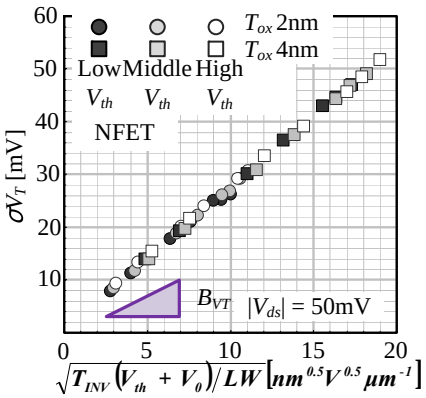

Fig.2 Takeuchi plot of MOSFETs for various kind of T_{INV} and N_{SUB}. (Reprinted from [2])

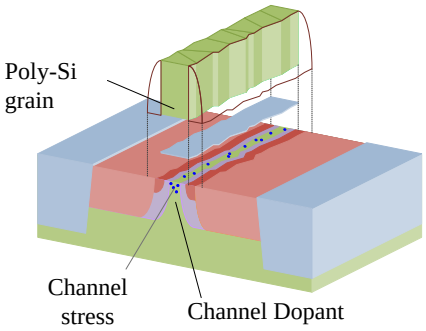

Fig.3 Candidate origins of V_T variability evaluated in this study.

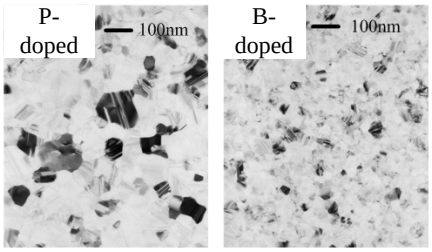

Fig.4 Grain structure of NFET nad PFET.

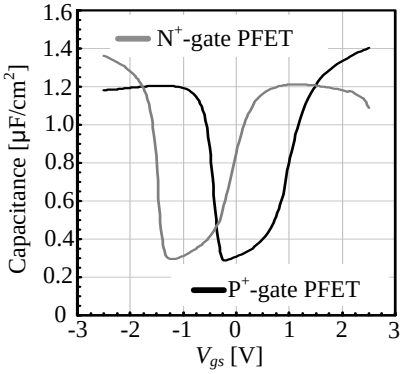

Fig.5 C-V characteristics of N+ gate PFET and P+gate PFET. Flat band voltage is shifted appropriately.

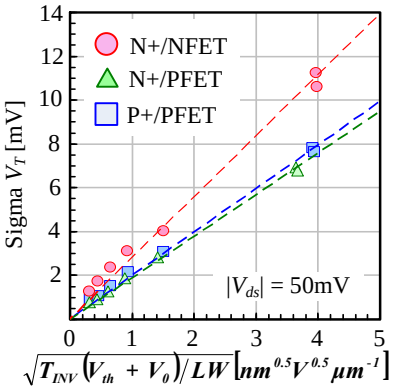

Fig.6 Takeuchi plot of N+gate NFET, N+gate PFET and P+gate PFET.

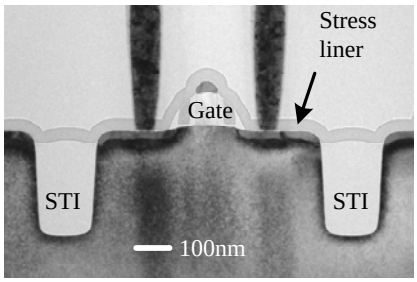

Fig.7 Cross sectional TEM image of MOSFET. Stress liner is used to controll channel stress.

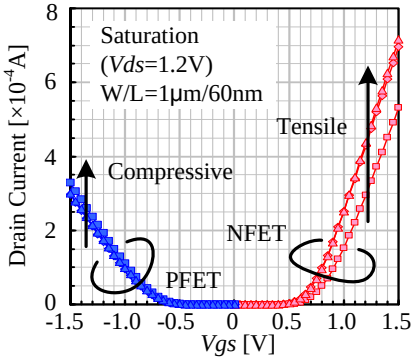

Fig.8 I_d-V_g characteristics of NFET and PFET with various stress liners.

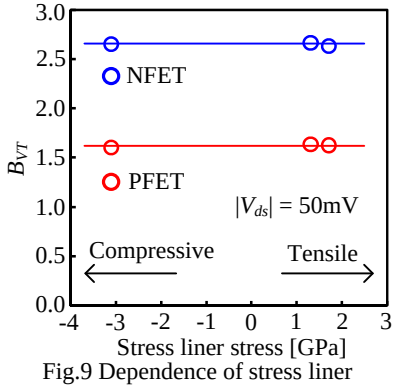

Fig.9 Dependence of stress liner condition on B_{VT}.

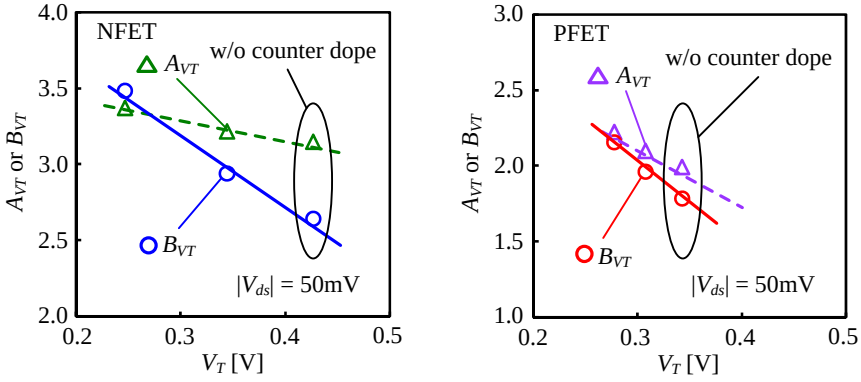

Fig.10 A_{VT} and B_{VT} of MOSFETs with counter dope.

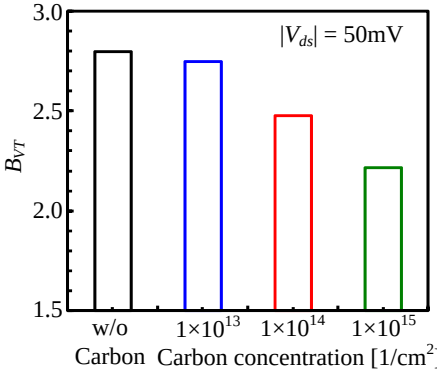

Fig.11 Dependence of halo carbon co-implantation condition on B_{VT}.