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Comprehensive Design Methodology of Extension Profile to Suppress Boron TED in High Performance High-k/Metal SiGe pMOSFETS

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Introduction

Since high-k/metal gate stacks have been successfully implemented in CMOS technology, alternative channels, such as SiGe and GaAs, have gained attention as a way to overcome roadblocks to performance enhancement [1-4]. SiGe devices are widely accepted as a performance booster in pMOSFETs because of their high hole mobility and good Si-based process compatibility.

So far, however, few systematic studies have been reported that address the physical mechanisms of boron diffusion in strained SiGe/Si heterojunction layers with different SiGe layer thicknesses and Ge contents (>50%), especially with high temperature annealing [5-7]. In addition, the effects of the fluorine incorporated during BF_2 implant on boron diffusion should be investigated to provide more insight into short channel device design. In this study, we investigate how short channel margins are affected by Ge mole fraction and SiGe layer thickness in a compressively strained SiGe/Si heterojunction PMOS with high temperature annealing. The role of fluorine in the short channel margin and reliability are also addressed.

Experiment

A compressively strained SiGe/Si channel and source/drain (S/D) PMOS was fabricated by a standard 45nm gate-first CMOS flow (Fig.1). A silicon capping layer was used for the compressively strained SiGe/Si channel and S/D PMOS. A control PMOS with a Si channel was also fabricated.

To study Ge effects on boron diffusion, epitaxial SiGe was grown by ultrahigh vacuum chemical vapor deposition (UHVCVD) using Si_2H_6 and GeH_4 on an n-type Si substrate with shallow trench isolation [8,9]. The thickness of the epitaxial SiGe layers ranged from 5nm~30nm and the Ge concentration ranged from 0~50%; the layers deposited were based on the critical thickness to control defects such as misfit dislocations as well as to minimize strain relaxation [10]. The implanted B profiles were characterized using secondary ion mass spectroscopy (SIMS).

In designing short channel pMOSFETs, devices with and without Ge PAI were fabricated with a BF_2 or B lightly doped drain (LDD). Detailed split conditions are summarized in table 1. All samples received the same spike anneal at 1070°C to maintain compatibility with Si CMOS processing.

RESULTS AND DISCUSSION

1. Effects of SiGe thickness and Ge concentration on LDD boron diffusion

Fig. 2 shows boron profiles in the Si and SiGe/Si substrates. For as-implanted profiles, both samples exhibit similar profiles and junction depths. For a longer annealing time at the same temperature, the B profile in the SiGe/Si become deeper, which is attributed to enhanced boron diffusion because B is less soluble in SiGe. Simulated boron profiles and junction depths using our calibrated simulation model matched the boron profiles and junction depths from SIMS analysis well (Fig. 3 and 4).

When the Ge concentration is increased, the threshold voltage (V_{th}) roll-off and drain-induced barrier leakage (DIBL) become more significant as shown in Fig. 5. For different SiGe thicknesses, V_{th} roll-off and DIBL degrade when t_{SiGe} increases (Fig. 6).

Table 2 and Fig. 7 exhibit simulated doping profiles and junction depths for different Ge concentrations and SiGe thicknesses. When the SiGe is thicker, the junction depth becomes deeper and the lateral diffusion of boron in the Si layer increases. The x_j and lateral diffusion are more significant when the Ge concentration increases. The reason for these deeper x_j and increased later diffusion is that the solubility of B in SiGe is less soluble. The dopant beyond the solubility limit can be ejected from the SiGe layer and enhance boron diffusion in Si. Therefore, a thicker SiGe layer can release more boron, resulting in deeper x_j. A greater Ge concentration also accelerates boron diffusion in Si because the boron is less soluble. These results can explain the V_{th} roll-off and DIBL in Fig. 5 and 6. Therefore, the optimum SiGe layer thickness and Ge concentration for short channel designs is <5nm and 25%, respectively. In terms of thermal stability, 25% SiGe is very compatible with Si-based CMOS processes.

2. Effects of dopant type and Ge PAI on short channel margin and reliability

For better short channel margins, we need to pay more attention to controlling the LDD boron profile because the 5nm thickness SiGe layer exhibits greater DIBL than the Si control devices. Ge PAI and different dopant splits (BF_2 and B) were used for device fabrication (Table 1). All split conditions show a similar range of equivalent oxide thickness (EOT) and interface trap density (N_{it}) (Fig. 8, and 9). Hole mobility improved 2.5x in all SiGe devices as shown in Fig. 10. For short channel device margins, Ge PAI devices exhibit better DIBL than devices without PAI (Fig. 11). Devices with a B LDD and Ge PAI show the best short channel margins among the split conditions. For devices with Ge PAI, improved drain breakdown voltage (BVDSS) was observed because of the better short channel margin (Fig. 12). These improved short channel margins resulted in better I_{on} at given DIBL and I_{on}-I_{off} characteristics (Fig. 13 and 14).

While the Ge PAI technique is effective with both BF_2 and B implants, the reason for the better short channel margin in B LDD devices both with and without Ge PAI is fluorine effect. A previous study found fluorine can enhance boron diffusion within amorphous Si when the F implant was performed separately [11]. Thereby, fluorine-induced B diffusion is mitigated for BF_2 implanted sample.

In terms of reliability, SiGe devices show less V_{th} shift at a given negative bias temperature instability (NBTI) stress while all samples show similar power-law dependence as seen in Fig.15 and 16. Fluorine from the BF_2 implant helps improve NBTI immunity. The BF_2 LDD with Ge PAI structures exhibit better NBTI immunity (less ΔV_{th} and ΔG_{mmax}), which suggests that Ge PAI may help retain more residual fluorine.

CONCLUSION

A systematic study was performed to understand the mechanism of boron diffusion in SiGe/Si substrates. To improve the short channel margins, SiGe thickness and Ge concentration should be carefully selected. In a given SiGe/Si substrate, Ge PAI can improve the short channel margin because boron diffusion is mitigated. There is a trade-off with fluorine effects in short channel margin and reliability characteristics.

Acknowledgements

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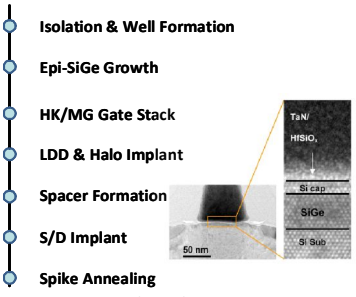


Fig. 1. Process flow for SiGe pMOS fabrication and TEM image of a final device structure

Table 1. Sample split conditions

	t_{SiGe}	Ge %	Ge PAI	LDD
CON	x	x	x	
Group 1	5nm ~ 30nm	25% ~ 50%	X	BF_2
Group 2	5nm	25%	X	BF_2
				B
			O	BF_2
				B

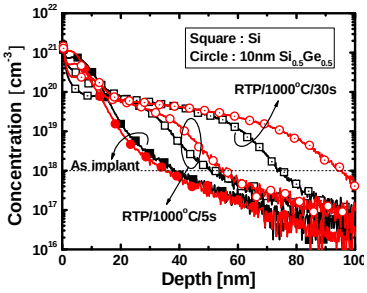


Fig. 2. Boron profile in Si and SiGe/Si substrate

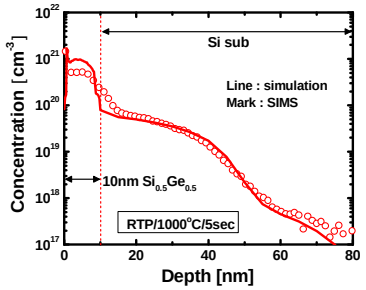


Fig. 3. Process simulation comparing SIMS profile.

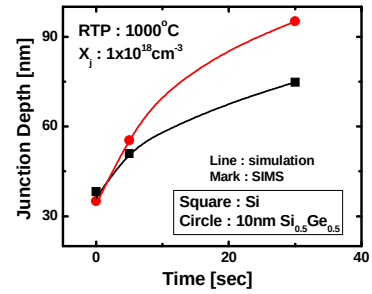


Fig. 4. Simulated and measured junction depth as a function of anneal time

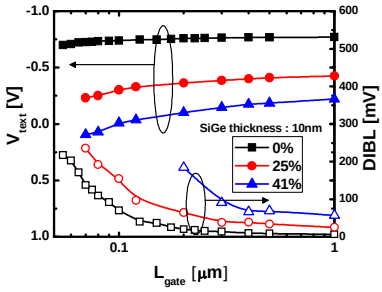


Fig. 5. Vth and DIBL for various Ge concentration. With increasing Ge %, short channel margin become smaller

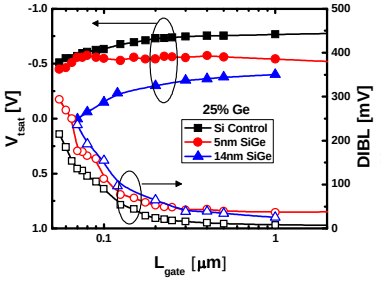


Fig. 6. Effect of SiGe thickness on V_{th} and DIBL. With increasing SiGe layer, V_{th} roll-off and DIBL become worse.

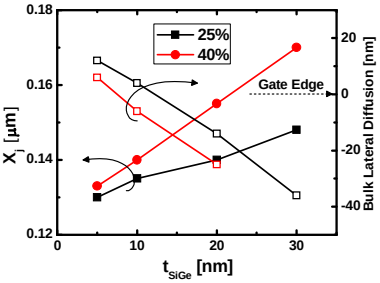
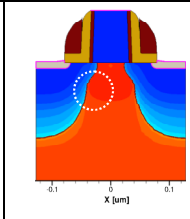
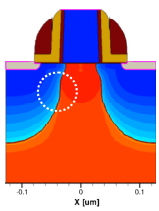
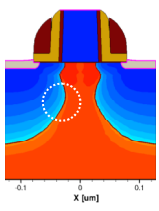
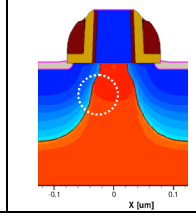
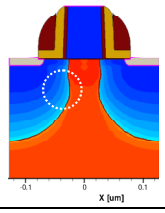
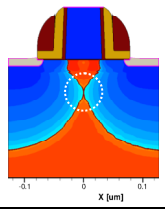


Fig. 7. With increasing SiGe thickness and Ge concentration, X_j and bulk boron lateral diffusion become greater due to transient boron diffusion.

Table 2. 2D doping profile of various SiGe thickness and Ge concentration

C_{Ge}\t_{SiGe}	5nm	10nm	20nm
25%			
40%			

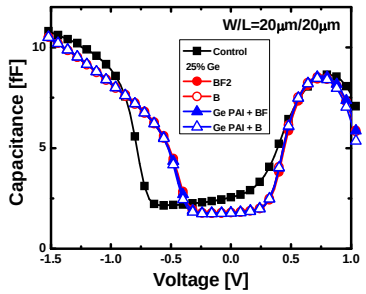


Fig. 8. All sample devices show similar EOT (=1.1nm).

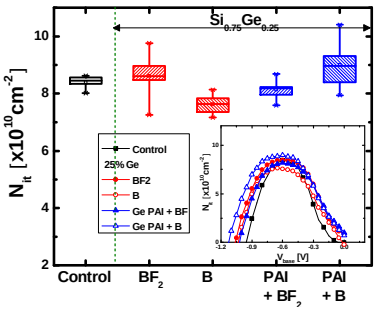


Fig. 9. All sample device exhibit similar N_{it}.

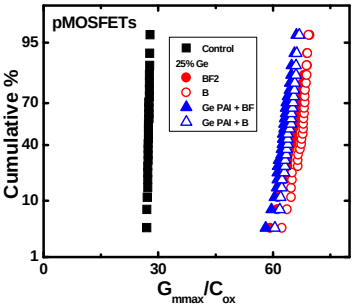


Fig. 10. 2.5x mobility enhancement for all SiGe devices comparing to the Si control devices.

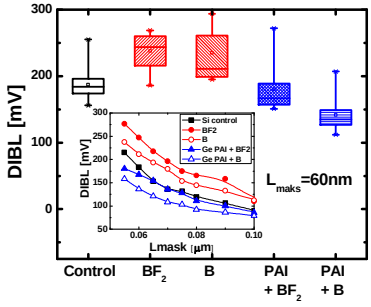


Fig. 11. With Ge PAI, DIBL become less comparing to w/o Ge PAI. B LDD exhibit lower DIBL indicating improved short channel margin.

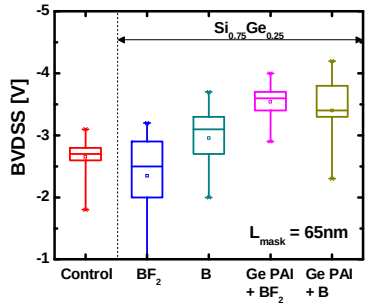


Fig. 12. Ge PAI samples show improved BVDSS comparing to the control and w/o PAI devices.

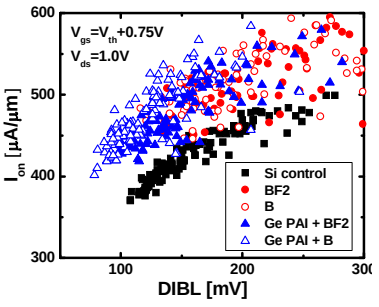


Fig. 13. SiGe devices exhibit improved output characteristics at a given DIBL. PAI + B LDD show the best result

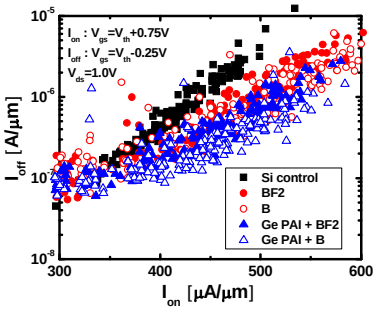


Fig. 14. Due to improved short channel margin, Ge PAI devices exhibit highest Ion at I_{off}=200nA/μm.

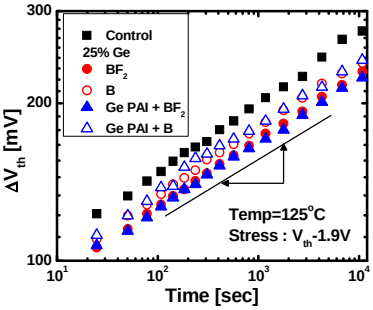


Fig. 15. All BF_2 implanted samples show less V_{th} shift due to fluorine effect. All samples show a similar slope.

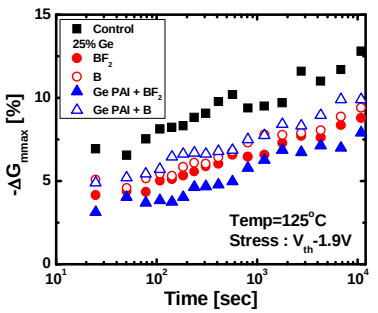


Fig. 16. Ge PAI may help retain more residual fluorine resulting in less G_m degradation.