Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1020-1021

On the Reliability of and Self-Compensation in Strained Transistors

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1. Introduction

Since the early days of semiconductor industry, the counterbalancing requirements of performance and reliability have defined the specifications of each successive CMOS technology nodes. In recent years, it has been difficult to scale the gate oxide thickness below 1nm due to gate leakage and off-state power-dissipation. Therefore, there has been a broad consensus in the industry that performance of the transistors can only be improved by using strained substrates or high-k dielectrics or a combination thereof. Many groups have studied the implications of this change in the substrate and the gate oxide regarding the classical reliability issues involving Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI), Hot Carrier Degradation (HCI), Gate Dielectric Breakdown (TDDB), *etc*.

Of these degradation mechanisms, the influence of strained substrate on NBTI performance has been most interesting, because there has been no broad consensus regarding the matter [1-7]. Moreover, there have been experiments demonstrating the counterintuitive notion that strain engineering may actually lead to self-compensating transistors that can not only reduce/eliminate the influence of NBTI degradation [8], but also suppress the V_T fluctuation arising from PBTI, distribution in gate oxide thickness as well as work-function differences. In this paper, we summarize our recent results regarding this topic.

2. NBTI Considerations in Strained Transistors

The classical theory of NBTI degradation attributes the time-dependent shift in threshold voltage (ΔV_T) to the depassivation of Si-H bonds at the Si/SiO_2 interface and subsequent diffusion of H/H_2 into the oxide/poly region [9]. Early ESR results by Stesmans et al. [10] suggested that the nature of defects does not change with strain, however, the number of bonds available for defect generation (N_0) increases (decreases) with compressive (tensile) strain. This increase in N_0 may reflect in poorer NBTI performance for compressively strained PMOS transistors, currently being used in CMOS technology. Subsequent experiments showed that the activation and field acceleration remain unchanged with strain [1-3, 11], but the NBTI degradation is often found to *decrease* with compressive strain [2, 5, 11], contradicting the ESR-based previous suggestions.

The puzzle of the NBTI degradation is resolved if one systematically explores the fundamentals of Si-H bond dissociation process via the R-D model (Fig. 1a), which suggest that the defects generated due to NBTI is given by: $N_{IT} \sim [N_0 P_T \exp(\gamma E_{ox})]^{2/3} t^n$; where, P_T is field-independent pre-factor for hole tunneling probability, γ is the field acceleration factor, $E_{ox} \sim (V_G - V_T)$ is the oxide electric field, and $n \sim 1/6$ is the field/temperature independent time exponent. Here, P_T depends – among other things – on the effective barrier height for hole tunneling (φ_{bh}) [11]. Our measurements show – and this is the key to the puzzle – that while γ does not change with strain, but at given E_{ox} the pre-factor P_T decreases (increases) with compressive (tensile) strain (Fig. 1b,c). This presumption of P_T reduction as being the source of NBTI improvement in compressively strained transistors is also supported by corresponding reduction in the leakage current (see [3, 11]), both of which are correlated via the increase in φ_{bh} (Fig. 1b). The interpretation of P_T-dictated change in ΔV_T is also consistent with increased NBTI degradation with bi-axial tensile strain (Fig. 1c). Once again, the field acceleration factors remains essentially unchanged with biaxial strain [1, 3].

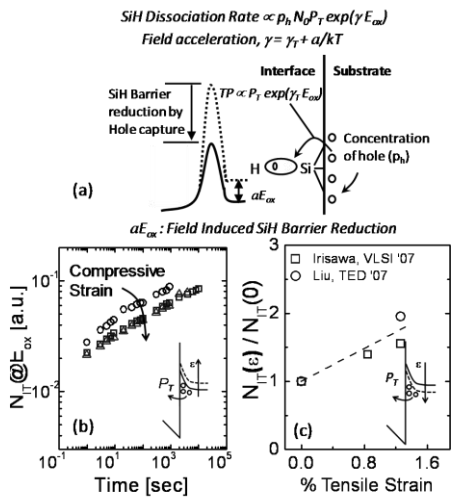

Fig. 1: (a) Universal view of Si-H bond dissociation under NBTI stress [9]. (b) Compressive strain decreases P_T due to increase in φ_{bh} (inset) and thus decreases $N_{IT}@E_{ox}$ [11]. (c) Tensile strain increases φ_{bh} and P_T (inset) and thus increases $N_{IT}@E_{ox}$.

3. On the Possibility of Degradation Free Transistors

It is well known that since $I_{D,lin} \sim \mu C_{ox}(V_G - V_T)$, the enhanced mobility (μ) of the strained channel would improve the drive-current (and therefore the performance) of a transistor. Less well appreciated is the implication of enhanced slope of the mobility-field (μ-E_{eff}) universal curve of the strained transistors in ameliorating the effects of charge trapping/trap-generation at the Si/SiO2 interface. It is easy to see that any change in $I_{D,lin}$ must be due to changes in

mobility and the inversion charge, i.e., $\Delta I_{D,lin}/I_{D,lin0} = \Delta\mu/\mu - \Delta V_T/(V_G-V_{T0})$; where the parameters with 0 subscripts indicate pre-NBTI stress values. When V_T changes by NBTI or PBTI degradation, so does the μ. For strained transistors having steep μ-E_{eff} characteristics, BTI degradation at constant V_G increases μ (Fig. 2) [8]. This is because at constant V_G, E_{eff} reduces due to BTI; and thus the increase in μ due to E_{eff} reduction can compensate the decrease in μ originating from additional coulomb scattering (mainly due to N_{IT} generation [12] during NBTI). Historically, however, the slope of the μ-E_{eff} curve for unstrained transistors was so shallow that, $\Delta\mu_{eff}$ was either negative or very small; hence could be neglected and researchers focused exclusively on ΔV_T as the source of $\Delta I_{D,lin}$. With the enhanced slope of μ-E_{eff} characteristics in strained transistors, however, the mobility enhancement may partially, if not completely (the effect is smaller in $I_{D,sat}$ compared to $I_{D,lin}$ [8]), cancel the effect of ΔV_T to keep constant I_D. In other words, after degradation fewer electrons move at faster velocity to keep the current the same. In sum, strain engineering can create a transistor that shows no I_D degradation, although the transistor is certainly not defect-free. The importance of such degradation-free transistor for logic circuits is obvious, although the transistors in SRAM cell may not directly benefit from such degradation-free characteristics.

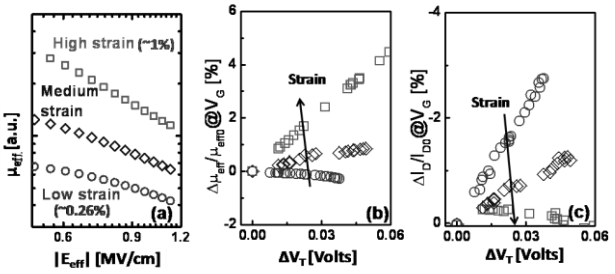

Fig. 2: (a) Presence of compressive strain increases the steepness of the μ-E_{eff} characteristics [8]. (b) Transistor with higher μ-E_{eff} steepness has more positive $\Delta\mu_{eff}$ @V_G due to NBTI stress, compared to the one having smaller μ-E_{eff} steepness. (c) Positive $\Delta\mu_{eff}$ @V_G in transistors having higher μ-E_{eff} steepness compensates the effect from ΔV_T and results negligible ΔI_D [8].

4. Strain and Self-Compensation of V_T Fluctuation

The SRAM transistors however would benefit from another aspect of strain-engineered self compensation that would improve the matching of the cells against thickness and work-function fluctuations. As is well known that the V_T of a transistor is given by –

$$V_T = \Phi_{MS} + \frac{T_{ox}}{\varepsilon_{ox}}\sqrt{4k_B T\varepsilon_{Si}N_D \ln\frac{N_D}{n_i}} + \frac{2k_BT}{q}\ln\frac{N_D}{n_i} + q\frac{\Delta N_T(t)}{C_{ox}} \quad (1)$$

where, Φ_{MS} is the metal-substrate work-function difference, T_{ox} is the dielectric thickness (referred to SiO_2), and $\Delta N_T(t)$ are concentration of charged defects (referred at the Si/SiO_2 interface). Once again, thicker oxides increase V_T, but reduce E_{eff}. As such, although the induced charge is reduced, the mobility is actually enhanced. Given an optimized strain-engineered channel, the two counterbalancing factors would keep I_D roughly the same independent of T_{ox}. It is easy to see that such self-compensation would apply to fluctuation in gate work-function as well. However, I_D fluctuation due to channel length variation (small for well designed DIBL-free transistors) and V_T fluctuation due to random-dopants (irrelevant for fully depleted structures) are not compensated and remain sources of I_D fluctuation.

An interesting consequence and external manifestation of the self-compensation between μ and V_T is the flatness of the I_D-V_G characteristics. Such flat characteristics may open up opportunities to eliminate guard-band voltages and reduce supply voltage (and power-dissipation) in the process. There are indications that various research groups have made substantial progress in this direction.

5. Conclusion

The importance of strain-engineering for high performance circuits is well known and broadly appreciated. In this paper, we highlight the additional opportunities of strain engineering in creating a technology that is inherently self-compensating against various reliability and V_T-fluctuation issues. The use of such degradation free technology would not only simplify IC design, but also help reduce the supply voltage (and power dissipation) by significantly curtailing the guard-band necessary to account for device-to-device parameter fluctuation.

Acknowledgements

We gratefully acknowledge NCN for computational resources, BNC for experimental facilities, and TSMC, AMAT, NCN for financial support for this work.

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