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Study of Negative V_{th} Shift in PBTI and Positive Shift in NBTI for Yttrium Doped HfO_2 Gate Dielectrics

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1. Introduction

Bias temperature instability (BTI) is one of the most serious issues for high-k gate dielectrics [1]. And rare earth doping technology into Hf-based oxide is attractive for V_{th} reduction in nMOSFETs [2]. There are several reports regarding the effect of such rare earth material doping on BTI [3-5]. These include reports that unusual V_{th} shift in PBTI has been observed in La or Dy doped high-k gate dielectrics [4-5]. Specifically, that is, negative shift occurred at lower fields, although positive shift was observed at higher fields. Although Yttrium is also effective for V_{th} reduction in nMOS [6], its impact on reliability has not been reported yet. This paper reports on the investigation of the PBTI and NBTI in Y doped high-k gate dielectrics, and observes that the opposite direction shift can be observed, not only in PBTI but also in NBTI, and that this unusual shift can be suppressed by nitrogen incorporation into the gate dielectrics.

2. Experimental

Fig.1 shows the sample fabrication flow in this study. Y_2O_3 was deposited with an ALD technique on HfO_2/SiO_2 or HfON/SiON. The number of deposition cycle of ALD varied from 2 to 10 cycles. (1.5E14 Y-atoms/cm^2 for each cycle) A post deposition anneal was carried out to diffuse Y into the gate dielectrics. PBTI and NBTI were measured at temperature from 25 to 125^{o}C.

3. Results and Discussion

PBTI

Fig. 2 shows the time evolution in PBTI of V_{th} shift of Y doped HfO_2. At low bias (1.4~1.6V) negative V_{th} shift occurred. On the other hand, at higher bias, positive shift due to the electron traps in bulk high-k was observed [1]. This negative shift was not observed for non Y doped HfO_2 gate dielectrics as shown in Fig. 3. We can say that this negative shift is due to the effect of Y incorporation. Fig. 4 shows the time evolution of V_{th} shift in PBTI with several concentrations of Y depositions. Positive shift was enhanced with increasing Y deposition amount of atoms. There are two candidate mechanisms for positive V_{th} shift in PBTI. One is hole traps, and the other is electron de-traps from high-k. Since an actual hole current is not injected into gate dielectrics [7], this negative shift is not due to hole traps, but to electron de-traps from high-k. For further understanding, we have checked the drain and gate leakage current behavior. Fig. 5 shows the gate leakage current (J_g) of an nMOS in inversion, with and without Y HfO_2 using carrier separation technique. Conduction and valence electron [7] currents were observed for both gate dielectrics. A kink was observed for valence electron in Y doped HfO_2. This indicates that some inner electric field change due to electron de-trap during IV sweep. Fig. 6 shows time evolution of the maximum of transconductance (G_m), normalized to the non stressed condition, at several stress voltages in PBTI. G_m enhancement is clearly observed at a 1.4V stress voltages, at which negative shift occurs. This indicates that the coulomb scattering factor was reduced in this region. Considering with this result, Y incorporation resulted in the gate dielectrics being charged negative, and this *Gm* enhancement stemmed from the charge neutralization by electron de-traps with voltage stress. Fig.7 shows the time evolution of V_{th} shift in PBTI at several temperatures. This negative shift was enhanced with rising temperature. Since hole traps are thought to be not so thermally active, this result assists the electron de-traps model. Our modeling of negative shift in PBTI is shown in Fig. 8. This Y related defect can be suppressed with nitrogen incorporation into the gate dielectric. Fig. 9 shows time evolution of V_{th} shift in PBTI for Y doped HfON gate dielectric. Negative shift can not be observed at any bias. Nitrogen incorporation suppresses this unusual V_{th} shift in PBTI.

NBTI

This opposite direction V_{th} shift was observed for not only PBTI but also NBTI. Fig. 10 shows time evolution of V_{th} shift in NBTI for Y doped HfO_2. Although the usual negative shift was observed at higher stress voltages (~ -1.8V), a slightly positive shift occurred at lower bias (~ -1.2V). This positive shift was not apparent for non Y doped HfO_2, as shown in Fig. 11. As with PBTI, this positive shift is due to electron traps or hole de-traps from high-k. It is very difficult to separate the effect of hole de-traps and electron traps, because both electrons and holes are injected into gate dielectrics of pMOS in inversion, in contrast to nMOS. Fig. 12 shows the gate leakage current with carrier separation, with and without Y incorporation. This indicates that Y incorporation changes the J_g component. Although dominant factor in J_g for non Y doped HfO_2 is holes, dominant component in Y doped HfO_2 changes to electrons. Considering the high electron component in J_g with the effect of Y doping, we speculate that this positive shift is due to the electron traps by the Y related defects (Fig.13) and the reason for electron current increase is thought to be due to the trap assisted tunneling through this Y related defect. This positive shift can be suppressed with N incorporation, as with PBTI, as shown in Fig.14.

4. Summary

We have studied the unusual V_{th} shift in PBTI and NBTI for Y doped HfO_2 gate dielectrics. Both stress conditions introduce the opposite shift for Y doped HfO_2 in the lower stress region. This is due to the Y related defects, with electron de-traps in PBTI and electron traps in NBTI. Such defect formation can be suppressed with N incorporation into HfO_2.

5. References

[1] S. Zafar *et al.*, J. Appl. Phys. 93 (2003) 9298, [2] P. Sivasubramani *et al.* :VLSI Symp. (2007) p.68, [3] M. Sato *et al.*, :IEDM (2008) p.119, [4] O'Sullivan *et al.*, JAP 044512 (2008), [5] S. Z. Chang *et al.*, 2008 VLSI Symp. p.62, [6] S. Kamiyama *et al.*, 2008 IEDM. p. 41, [7] M. Sato *et al.*, JJAP 46 (2007) 1058,

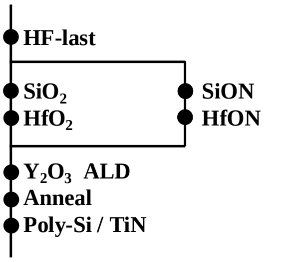

Fig.1 Sample fabrication flow.

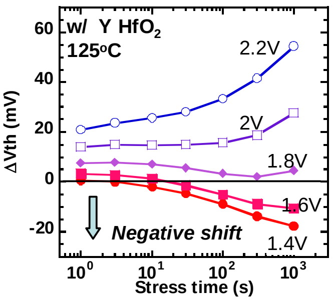

Fig.2 Time evolution of ΔV_{th} in PBTI under several voltages of Y doped HfO_2. negative V_{th} shift was observed at lower fiels.

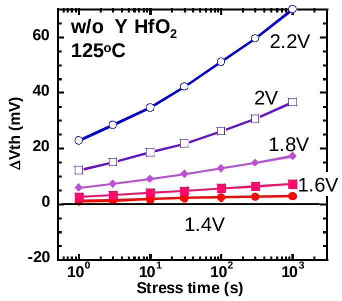

Fig.3 Time evolution of ΔV_{th} in PBTI under several voltages . Negative V_{th} shift was not observed.

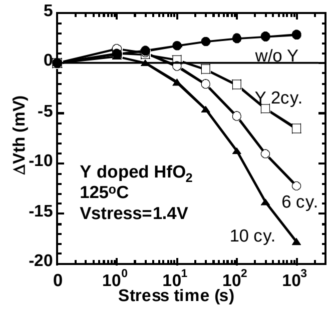

Fig.4 Time evolution of ΔV_{th} in PBTI with several amount of doped Y. With increasing Y incorporation, negative V_{th} shift was accelerated.

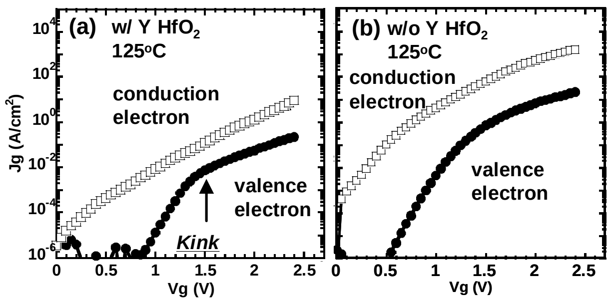

Fig.5 Gate leakage current of (a)Y doped and (b) non doped HfO_2 nMOS measured with carrier separation. Kink in valence electron current was observed for Y doped HfO_2.

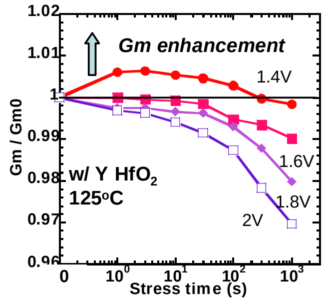

Fig.6 Time evolution of $G_{m\text{-}max}$ in PBTI under several voltages. At low voltage, G_m enhancement was observed.

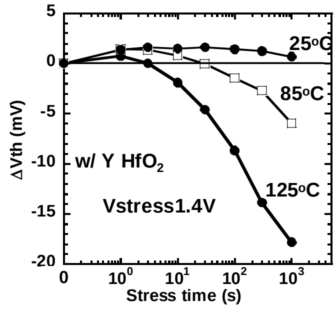

Fig.7 Time evolution of ΔV_{th} in PBTI at several temperatures. With rising temperature, negative V_{th} shift was accelerated.

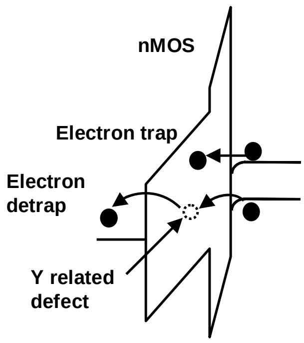

Fig.8 Schematic of PBTI of Y doped HfO_2. At low field, electron de-trap is dominant in PBTI compared to electron traps.

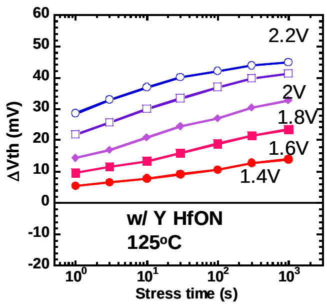

Fig.9 Time evolution of ΔV_{th} in PBTI under several voltages for Y doped HfON. Negative V_{th} shift was not observed.

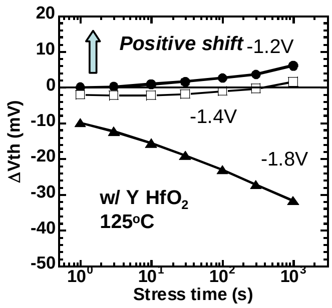

Fig.10 Time evolution of ΔV_{th} in NBTI under several voltages for Y doped HfO_2. Positive V_{th} shift was observed at lower bias(-1.2~-1.4V).

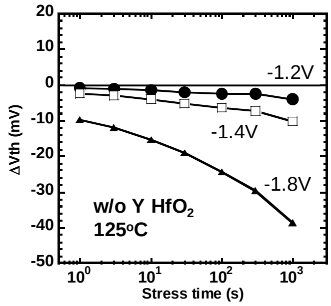

Fig.11 Time evolution of ΔV_{th} in NBTI under several voltages of HfO_2. Positive V_{th} shift was not observed.

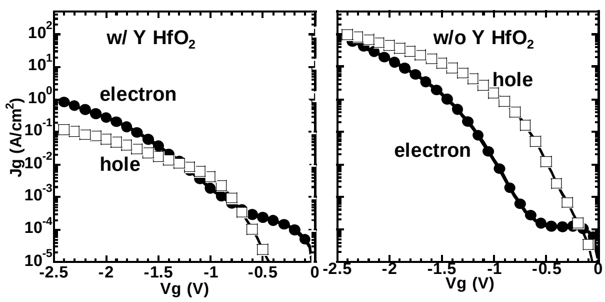

Fig.12 Gate leakage current of pMOS measured with carrier separation. (a) Y doped HfO_2, (b) Y non doped HfO_2 When Y was doped, dominant carrier component in *Jg* was electrons. While, hole is dominant for non Y doped HfO_2

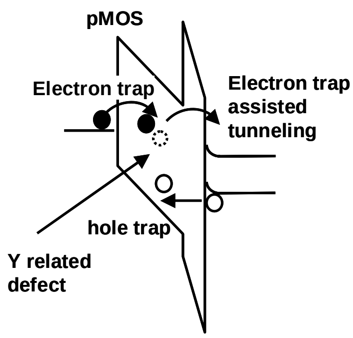

Fig.13 Schematic of NBTI of Y doped HfO_2. At low field, electron trap is dominant compared to hole trapping.

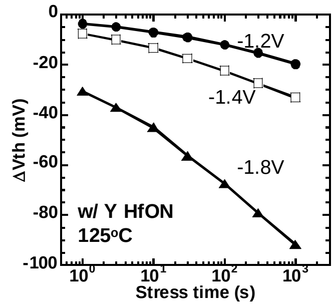

Fig.14 Time evolution of ΔV_{th} in NBTI under several voltages of Y doped HfON. Positive V_{th} shift was suppressed.