Forward Body Bias Enhanced NBTI Recovery on pMOSFETs

Yandong He, Gang Du, YunXiang Yang, Ganggang Zhang

Institute of Microelectronics, Peking University
Beijing 100871, P. R. China
Phone: +86-10-62767915-ext802 E-mail: heyd @pku.edu.cn

1. Introduction

Forward body bias (FBB) has been considered as a promising approach for extending the scalability of bulk-Si MOSFET in the era when gate oxide can not be scaled down further[1-2]. When the sub-2nm gate oxides have to incorporate more and more nitrogen to suppress the gate leakage current, the negative bias temperature instability (NBTI) has become the most crucial reliability issue[3]. The extensive studies have been made on NBTI degradation and recovery mechanism[4-7]. Up to now, more attention on recovery was focused on the gate bias and dynamic frequency dependence[5-7], few effort was put on the effect of body bias on the NBTI recovery. As the introducing the FBB into CMOS integrated circuit design, such as the dynamic Vt MOSFET (DTMOSFET), the exploration on NBTI recovery under FBB is necessary, which will help to understand and evaluate the FBB technique. In this paper, we report a detailed experimental study of NBTI recovery under typical application condition for DTMOSFET, i.e., \( V_g = V_b \). Our results show that not only the positive gate bias but also the FBB will enhance the recovery of NBTI for pMOSFET. Therefore, the forward body biasing can improve the drive capability without degrading the NBTI lifetime.

2. Devices and Experiments

The devices used in this study were \( p^+ \) polysilicon gate p-MOSFETs with equivalent oxide thickness of 1.7nm oxynitride gate oxide. In order to investigate the NBTI recovery, the identical stress was used in this study unless otherwise specified explicitly. The stress was kept at \( V_g = -2.0V \), the other terminals were grounded. In the recovery stage, not only the gate but also body bias is varied accordingly. The relative variation of \( \frac{\Delta I_d}{I_{d0}} \) and \( \frac{\Delta V_{th}}{V_{th0}} \) was used as a characteristic monitor to avoid the device-to-device variation.

3. Results and Discussion

Once the magnitude of gate voltage is lower than NBTI stress voltage, the device parameters shift will reduce to some extend. The evolutions of \( \frac{\Delta I_d}{I_{d0}} \) during stress and recovery phase were shown in Fig. 1. The decrease of \( \frac{\Delta I_d}{I_{d0}} \) followed the power law with a power exponent of 0.211, shown in the inst of Fig1. It is consistent with the R-D model prediction[6]. The recovery rate was defined as the relative change of \( \frac{\Delta I_d}{I_{d0}} \) in percentage from the total degradation at \( V_g = -2.0V \).

It is seen that the corresponding recovery rates are 18.9%, 58.8% and 85.7%, respectively. The device can recover about 40% more at FBB of -1.0V than that of \( V_g = -1.0V \), which indicates that recovery is efficient under FBB condition. The oxide field was same under FBB and zero body bias. Therefore the enhanced recovery cannot be attributed to the field-dependent reverse reaction rate.

In Fig.2, it is seen that the degradation of \( G_{\text{max}} \) and \( V_{th} \) shift induced by the stress and variable recovery has a linear relationship. This indicated that the NBTI generated traps recovered at the same reverse trend regardless of the recovery bias conditions.

By the same methodology, we study the dependency of recovery rate on the recovery bias, shown in Fig.3. It is obvious that the recovery rate differs with the magnitude and polarity of the recovery gate voltage and/or body bias voltage. At negative gate bias, a weak dependence of the
recovery rate was observed. However, at FBB bias condition for $|V_g|=|V_b| \leq 0.8V$, the recovery rate increases with an increase of FBB, which produces larger recovery compared to the gate only recovery condition. A further increase of body bias barely affect recovery rate, resulting in a saturated recovery rate. The recovery for $|V_g|=|V_b| \geq 0.8V$ was saturated because of the voltage drop on the substrate series resistance due to the large forward bias current, resulting in a nearly constant body bias voltage.

In Fig.6, typical AC stress and FBB AC stress results are compared. At a given time of stress, the FBB AC stress degradation is lower than typical AC stress. The relative $I_{dsat}$ change after 10000s of FBB AC stress was about 30% lower than that of typical AC stress. In term of the lifetime at 10% $I_{dsat}$ shift, the FBB AC condition can achieve one order of magnitude increment.

The electron and hole density distribution (Fig.4) was simulated under FBB condition compared with zero body bias case. Near the Si/SiO$_2$ interface, a larger electron density was present under FBB condition. The possibility for interface trap and/or near interface bulk charge passivation assisted by free electrons will increase. The strong correlation between the shift of $G_{max}$ and the gate current (LVSILC, known as low voltage stress induced leakage current [8]) under positive gate bias recovery at 1.0V, which is just around the flat-band voltage for our technology, also suggested the mechanism of the band edge defects neutralization by electrons near Si/SiO$_2$ interface, shown in Fig.5.

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