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The Simulation of ESD Protection Devices Fabricated in Multiple-Gate FETs

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1. Introduction

Multiple-Gate FET (MuGFET) technologies such as FinFETs or nanowire MOSFETs are promising candidates for future CMOS devices [1] [2]. In these technologies, in order to adopt processes in common with the logic circuits, the electrostatic discharge (ESD) protection devices must also be fabricated in MuGFETs [3] [4]. We have examined the basic behaviors of FinFET-shaped ESD protection devices by device simulation. This work has revealed that some properties are different from those of planar type devices. Consequently, it is important to design circuits, taking these inherent properties into consideration.

2. Device Structure and Simulation Conditions

The device structure is illustrated in Fig.1. The gate length is 400nm, the gate-oxide thickness is 6nm, total height of FinFET (H) is 400um and the Si thickness (Tsi) ranges from 5nm to 100nm. The doping concentration in the n-type diffusion layer and the p-type substrate (Nch) is $7x10^{19}cm^{-3}$ and $1x10^{15}cm^{-3}$, respectively. Both gate electrodes are grounded and the input discharge pulse corresponds to 200V Machine Model.

It has been revealed that the quantum confinement effect modulates threshold voltage and drain current [5] [6]. The ESD simulation in this work indicates that the quantum confinement effect also modulates the trigger voltage (Vt1) or the holding voltage (Vh) owing to the relaxation of the electric field or the rise in the internal impedance, as shown in Fig.2 and Fig.3. However, shifts of drain contact voltage are small in comparison with the classical Vt1 and Vh. Consequently, ESD protection behaviors could be sufficiently examined by the classical model in ESD simulation.

3. Simulation Results and Discussions

With regard to the planar devices, gate length, thickness of gate-oxide, device layout and impurity concentration are design factors related to ESD protection behaviors. In addition to these factors, Vt1 and Vh are controlled by Tsi and H. Fig.4 shows the dependence of ESD protection behaviors on Tsi. Vt1 is dependent on Tsi and has a minimum value at Tsi = 20nm. This property is interpreted in terms of the electric field near the gate edge. Fig.5 indicates surface potential profiles when contact voltage reaches 3V. Potential in the channel is more influenced by the grounded gate bias as Tsi is reduced, namely, the electric field between the channel and the drain region becomes increasingly strong. Therefore, the avalanche breakdown is enhanced and Vt1 is reduced in the 100nm to 20nm range. On the other hand, the drain region is depleted under the condition that Tsi is less than 20nm. The depletion relaxes the electric field and it adversely increases Vt1. Fig.6 shows the dependence of ESD protection behaviors on H. Vt1 is decreased with the increasing of H. In fully depleted FinFETs, currents flow along not only the surfaces but also the center of the FinFETs (y=0 in Fig.1). Unlike DC bias conditions, the increasing of H raises the ratio of the current along the center to the total current owing to lower potential barrier. The current along the center flows like punch-through current and rarely generates the avalanche breakdown. Therefore, the increasing of H apparently induces the lowering of Vt1. On the other hand, Vt1 is independent of W with the planar devices as shown in Fig.7, where W corresponds to H in FinFETs. That is because the channel region is not fully depleted. Consequently, Vt1 in the FinFETs shows different behaviors toward the widening of Tsi or the increase of H as illustrated in Fig.8 and Fig.9.

Fig.10 shows the ratio of Vh to Vt1. The ratio is affected by Tsi or H because of the channel depletion or the current flowing along the center. Though it has also been revealed that the ratio is described as a function of the Gummel number [7], the ratio doesn't keep constant assuming that the volume of p-type substrate is fixed.

Nch is another design factor related to ESD protection behaviors as illustrated in Fig.11. Since the gate electrode surrounds the channel regions with the FinFETs, snapback could appear with low doping concentration, whereas the planar devices doesn't operate as ESD devices in the Nch=$1x10^{15}cm^{-3}$ to $1x10^{16}cm^{-3}$ range.

Regarding the application of FinFETs as ESD protection devices, there is a potential issue concerning high thermal resistance. Fig.12 shows the lattice temperature near the gate edge. The rate of the rise in lattice temperature could increase in comparison with the planar devices. The increase of H is more effective for suppressing the rise in lattice temperature than the widening of Tsi, since Vh is lower.

4. Conclusions

We have carried out the ESD simulation and revealed the fundamental properties of the FinFET-shaped ESD protection devices. It is clarified that Tsi and H are inherent design factors in the FinFET devices and have considerable effects on ESD protection behaviors. In addition, the FinFETs could operate as ESD devices in wide-range Nch. Though the high thermal resistance is a potential issue, the increase of H could suppress the rise in lattice temperature.

The FinFET-shaped ESD protection devices expand the possibility of I/O circuit design, utilizing these properties.

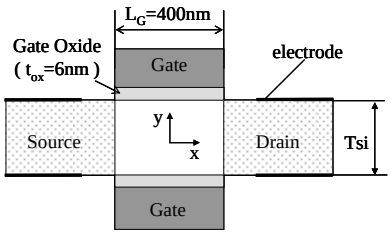

Fig.1: The device structure used in this simulation. Diffusion layers have abrupt junctions. Coordinate origin is set as indicated above.

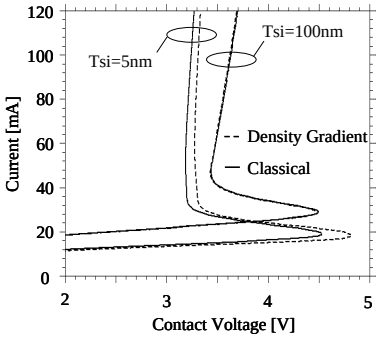

Fig.2: The quantum confinement effect on ESD protection behaviors.

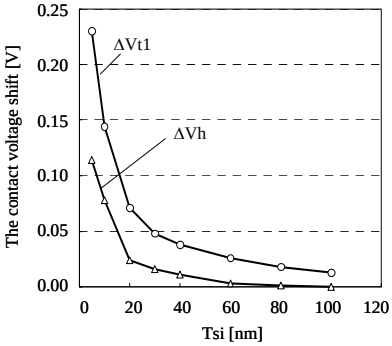

Fig.3: Shifts of the drain contact voltage owing to the quantum confinement effects.

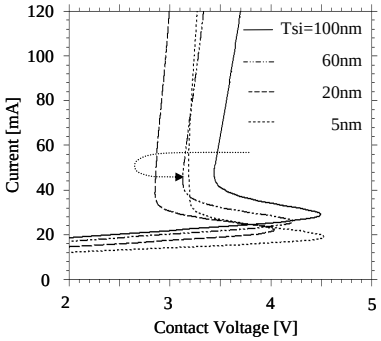

Fig.4: The dependence of ESD protection behaviors on Tsi.

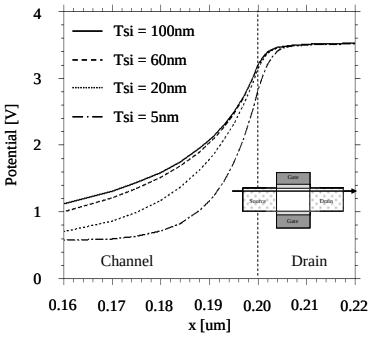

Fig.5: Surface potential profiles when contact voltage reaches 3V.

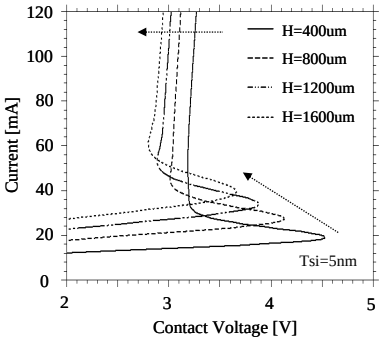

Fig.6: The dependence of FinFET-shaped ESD protection behaviors on W.

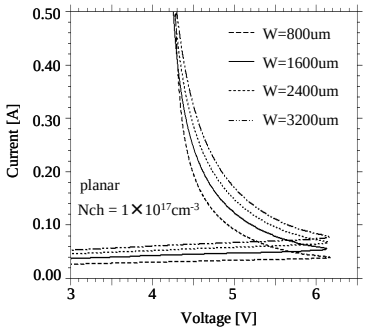

Fig.7: ESD protection behaviors in planar ESD protection devices

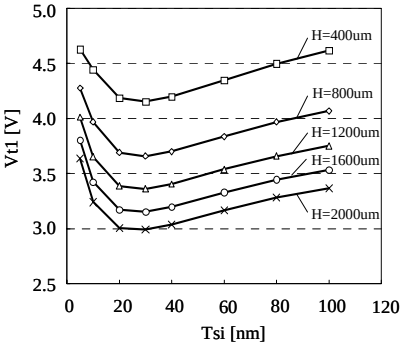

Fig.8: The Vt1 characteristics focused on Tsi.

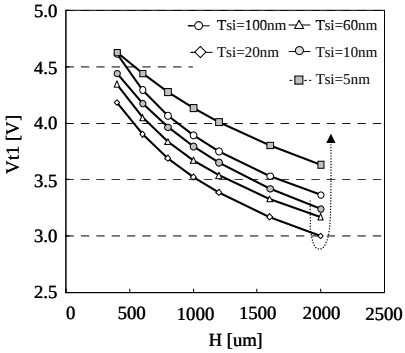

Fig.9: The Vt1 characteristics focused on W.

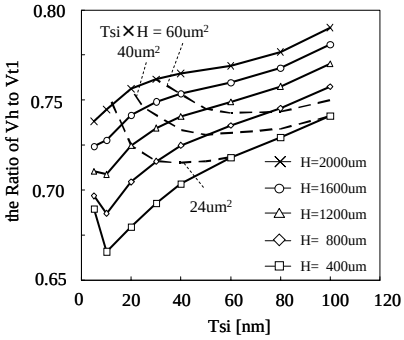

Fig.10: The ratio of Vh to Vt1 in FinFET-shaped devices. The dashed lines show the ratio with "Tsi x W = const".

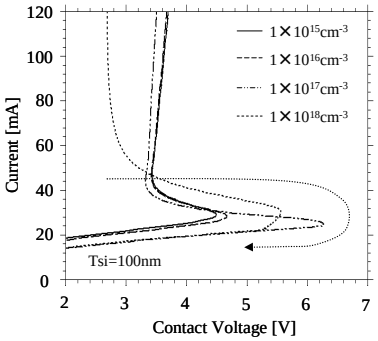

Fig.11: The dependence of ESD protection behaviors on Nch at Tsi=100nm

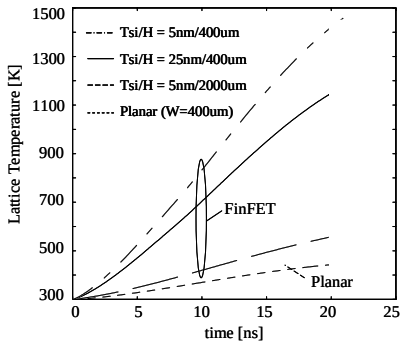

Fig.12: Lattice temperature in the FinFET-shaped devices near the gate edge.
FinFET: Nch=1x10^{15}cm^{-3}, Planar: Nch=1x10^{17}cm^{-3}

Reference [1]:H. Kawasaki et al., IEDM 2008, [2]: K. D. Buddharaju et al., Solid-State Electronics 52 (2008), p1312, [3]: C. C. Russ et al., IEEE Device and Materials Reliability, vol.7, no.1, 2007, p152, [4]: S. Thijis et al., IEEE Electron Devices, vol.55, no.12, 2008, [5]: M. G. Ancona et al, Phys. Rev. B, vol. 39, no.13, p9536, 1989, [6]: S. Odanaka, IEEE Trans. Computer-Aided Design of Integr. Circuits Syst., vol.23, issue 6, p837, June 2004, [7]: M. Sze, Physics of Semiconductor Devices, John Woley & Sons, New York, 1981