Wireless CMOS TSV

Tadahiro Kuroda

Keio University, Japan

kuroda@elec.keio.ac.jp

Abstract – Short-rage wireless communication technology has been widely applied. In the ubiquitous era, applications for connecting things have been expanding. When communication range is shorter than 1/10 of its wave length, the electromagnetic field shows unique characteristics of near field. For instance, inter-chip wireless communication of chips that are stacked in a package is the near-field communication. Wireless TSV employing inductive coupling bares comparison with TSV in performance with much inexpensive cost (Fig. 1). Application researches with industry have started after fundamental research in academia. For instance, SSD (Solid-State Drive) in a package can be realized by stacking NAND Flash memories. By changing number of processor chips in stacking according to required performance, one design can cover wide ranges of applications. A high-speed low-power link between a processor and a memory can be implemented. Inductive coupling inter-poser for rewiring coils with offset in position is also investigated. Extension of communication rages to millimeter ranges makes it possible to probe internal bus data through package for debugging and to perform non-contact wafer simultaneous testing. Wireless power delivery by using inductive coupling will further widen the applications. In this paper technology and applications of the wireless CMOS TSV are presented.

Chip performance improves 70% per year by device scaling. In order to fully utilize the performance improvement, signal bandwidth to/from a chip should be improved by 44% annually. Device scaling, however, provides with only 28% increase in the signal bandwidth. Innovations in communication schemes and circuits have kept the 44% improvement, but this approach is facing limitation. Brute-force acceleration of circuits have resulted in rapid increase of power dissipation in I/O [8]. TSV (Through Silicon Via) that can utilize area, not just periphery, is receiving attractions. TSV, however, is expensive and leaves reliable issues in manufacturing. A proposal of replacing TSV with a wireless transceiver, and moving from mechanical to electrical approach was made [8]. Near-field wireless communication is employed.

Regions that are shorter than a distance of wavelength divided by 2π is called near field [13-15]. In the near field electromagnetic waves receive strong attenuation that is in proportion to power of 3 of the distance. Therefore, when arranging communications channel in high density, there is very little crosstalk [3]. By this feature, inter-chip data link in SiP can be suitably made. Especially, wireless TSV by using inductive coupling is attracting attention.

We have been investigating wireless TSV and presenting research achievements every year in ISSCC since 2004 [1, 4, 6, 12, 20, 24, 25, 26], in the Symposium on VLSI Circuits [2, 7, 27, 28, 29, 30], and in SSDM [5, 9, 10, 16, 21]. It bares comparison with TSV in performance. Data rate per coil is 11Gb/s/ch [20]. Energy consumption is 0.14pJ/b [12],
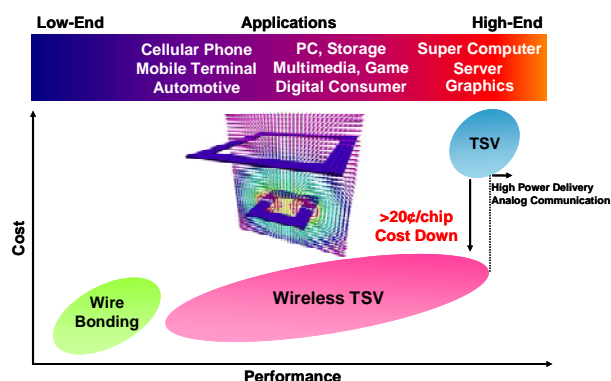

Fig. 1 Wireless TSV, inexpensive but comparable performance.

which is two orders of magnitude smaller than that of the conventional high-speed memory links such as DDR. Layout area is small and chip stacking is short. Reliability of communication is as high as wired communications.

By enlarging coil size, communications range extends [8]. Eddy current reduces strength of the inductive coupling when power mesh lines are placed in between coils [19], but that can be compensated by increasing transmission power [19]. The coil can be placed above SRAM memory cell array without problem [19]. Since inductive coupling provides with AC coupling, chips can be connected even under different DC voltages [8].

Furthermore, by thinning chip thickness, changes of magnetic field in the inductive-coupling link can be

1

maintained constant, and cost-performance ratio will be improved exponentially [8, 9].

Wireless TSV reduces cost for manufacturing by more than 20-cents per chip than TSV (Fig. 1), because wireless TSV is a digital CMOS circuit solution in a standard CMOS technology. Performance, on the other hand, is comparable with TSV. A large coil may be needed for long communication rages, but it can be placed above SRAM cell area to pose negligibly small impact in layout. An ESD protection device is not needed since wireless TSV needs no contact. Power, delay as well as layout area is reduced. AC coupling makes interface design quite simple under multiple/variable power supplies. Thinning chip thickness leads to exponential improvement in performance-cost ratio [8].

Wireless TSV for SiP applications is now a practical level. 64 chips of NAND Flash memory can be stacked in a package for an SSD (Solid-State Drive) in a package [24]. 4 chips of dynamic reconfigurable processor are stacked [28]. High-speed link between a commercial-level processor and a memory is verified in system level [26, 27]. An inductive-coupling interposer connects chips whose coils are placed non-concentrically [29].

There are research achievements other than SiP applications. Non-contact wafer testing is possible for cost reduction [25]. Internal bus data can be probed for debugging through a package [23]. Furthermore, power delivery by inductive coupling [16, 17] allows seal-up of a Mask ROM, resulting in 1000 year preservation of digital data [30].

REFERENCES

[1] D. Mizoguchi, *et al.*, "A 1.2Gb/s/pin Wireless Superconnect Based on Inductive Inter-chip Signaling (IIS)," *ISSCC*, pp.142-143, Feb. 2004.

[2] N. Miura, *et al.*, "Analysis and Design of Inductive Coupling and Transceiver Circuit for Inductive Inter-Chip Wireless Superconnect," *Symposium on VLSI Circuits*, pp. 246-249, Jun. 2004.

[3] N. Miura, *et al.*, "Cross Talk Countermeasures in Inductive Inter-Chip Wireless Superconnect," *CICC*, pp.99-102, Oct. 2004.

[4] N. Miura, *et al.*, "A 195Gb/s 1.2W 3D-Stacked Inductive Inter-Chip Wireless Superconnect with Transmit Power Control Scheme," *ISSCC*, pp.264-265, Feb. 2005.

[5] D. Mizoguchi, *et al.*, "Measurement of Inductive Coupling in Wireless Superconnect," *SSDM*, pp.670-671, Sep. 2005.

[6] N. Miura, *et al.*, "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," *ISSCC*, pp.424-425, Feb. 2006.

[7] M. Inoue, *et al.*, "Daisy Chain for Power Reduction in Inductive-Coupling CMOS Link," *Symposium on VLSI Circuits*, pp.80-81, Jun. 2006.

[8] T. Kuroda, *et al.*, "Perspective of Low-Power and High-Speed Wireless Inter-Chip Communications for SiP Integration," *ESSCIRC*, pp.3-6, Sep. 2006.

[9] D. Mizoguchi, *et al.*, "Constant Magnetic Field Scaling in Inductive-Coupling Data Link," *SSDM*, pp. 606−607, Sep. 2006.

[10] K. Niitsu, *et al.*, "60% Power Reduction in Inductive-Coupling Inter-Chip Link by Current-Sensing Technique," *SSDM*, pp.64-65, Sep. 2006.

[11] N. Miura, *et al.*, "A 1Tb/s 3W Inductive-Coupling Transceiver Chip," *ASPDAC*, pp.92-93, Jan. 2007.

[12] N. Miura, *et al.*, "A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping," *ISSCC*, pp.264-265, Feb. 2007.

[13] H. Ishikuro, *et al.*, "An Attachable Wireless Chip-Access Interface for Arbitrary Data Rate Using Pulse-Based Inductive-Coupling through LSI Package," *ISSCC*, pp.266-267, Feb. 2007.

[14] T. Kuroda, "CMOS Proximity Wireless Communications for SiP Integration (Invited)," *ISSCC*, Feb. 2007.

[15] H. Ishikuro, *et al.*, "Wideband Inductive-coupling Interface for High-performance Portable System," *CICC*, pp.13-20, Sep. 2007.

[16] Y. Yuxiang, *et al.*, "Chip-to-Chip Power Delivery by Inductive Coupling with Ripple Canceling Scheme," *SSDM*, pp. 502-503, Sep. 2007.

[17] Y. Yuxiang, *et al.*, "Non-Contact 10% Efficient 36mW Power Delivery Using On-Chip Inductor in 0.18mm CMOS," *A-SSCC*, pp.115-118, Nov. 2007.

[18] Y. Yoshida, *et al.*, "A 2Gb/s bi-directional inter-chip data transceiver with differential inductors for high density inductive channel array," *A-SSCC*, pp.127-130, Nov. 2007.

[19] K. Niitsu, *et al.*, "Interference from Power/Signal Lines and to SRAM Circuits in 65nm CMOS Inductive-Coupling Link," *A-SSCC*, pp.131-134, Nov. 2007.

[20] N. Miura, *et al.*, "An 11Gb/s Inductive-Coupling Link with Burst Transmission," *ISSCC*, pp.298-299, Feb. 2008.

[21] K. Niitsu, *et al.*, "Misalignment Tolerance in Inductive-Coupling Inter-Chip Link for 3D System Integration," *SSDM*, pp.86-87, Sep. 2008.

[22] K. Niitsu, *et al.*, "A 65fJ/b Inductive-Coupling Inter-Chip Transceiver Using Charge Recycling Technique for Power-Aware 3D System Integration," *A-SSCC*, pp.97-100, Nov. 2008.

[23] S. Kawai, *et al.*, "A Real-Time On-Chip Bus Trace System Using Quasi-Synchronous Inductive Coupling Transceiver," *A-SSCC*, pp.113-116, Nov. 2008.

[24] Y. Sugimori, *et al.*, "A 2Gb/s 15pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking," *ISSCC*, pp.244-245, Feb. 2009.

[25] Y. Yoshida, *et al.*, "Wireless DC Voltage Transmission Using Inductive-Coupling Channel for Highly-Parallel Wafer-Level Testing," *ISSCC*, pp.470-472, Feb. 2009.

[26] K. Niitsu, *et al.*, "An Inductive-Coupling Link for 3D Integration of a 90nm CMOS Processor and a 65nm CMOS SRAM," *ISSCC*, pp.480-481, Feb. 2009.

[27] K. Osada, *et al.*, "3D System Integration of Processor and Multi-Stacked SRAMs by Using Inductive-Coupling Links," *Symposium on VLSI Circuits*, pp.256-257, Jun. 2009.

[28] Y. Kohama, *et al.*, "A Scalable 3D Processor by Homogeneous Chip Stacking with Inductive-Coupling Link," *Symposium on VLSI Circuits*, pp.94-95, Jun. 2009.

[29] S. Kawai, *et al.*, "A 4.7Gb/s Inductive Coupling Interposer with Dual Mode Modem," *Symposium on VLSI Circuits*, pp.92-93, Jun. 2009.

[30] Y. Yuxiang, *et al.*, "Digital Rosetta Stone: A Sealed Permanent Memory with Inductive-Coupling Power and Data Link," *Symposium on VLSI Circuits*, pp.26-27, Jun. 2009.

2