Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp64-65

Design of On-Chip High Speed Interconnect on CMOS 180nm Technology

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1. Introduction

On-chip high speed interconnect technology is the emerging technology to improve the latency and the bandwidth of the on-chip data transfer across the processor chip die. There are various new proposals from researchers [1][2][3], however, there is no standard technique of this technology, and not many of the earlier researches address the optimal design method of this circuit technology.

In this paper, we describe the design method of the on-chip high speed interconnect. The circuit topology we propose is the differential serial link with the open drain TX driver, and the self-biased RX differential amplifier. The very compact equalization circuit is added to enhance the performance. The paper focuses mainly on how to optimize the equalization circuit.

2. Implementation and Design Methodology

We propose the on-chip high speed differential serial link, with the open drain TX driver, and the self-biased RX differential amplifier, shown in **Fig. 1**. Since on-chip interconnect has the high resistivity and relatively short flight time, the topology without the termination at the driver side should be suitable. It introduces the significant reduction of the current and capacitive load as compared with CML and LVDS driver. Lower loading leads to the smaller driver, which reduces the number of the pre-driver stages to accomplish the lower jitter and better performance. Very compact equalization circuit was implemented to RX, as shown in **Fig. 2,** which is conceptually the 2nd order IIR filter. Letting the transfer function of the interconnect $T_{TLINE}(\omega)$, and letting that of RX amplifier $T_{AMP}(\omega)$, the transfer function for the interconnect + RX amplifier + equalizer can be written as follows:

$$\text{Transfer Function} = \frac{T_{TLINE}(\omega)T_{AMP}(\omega)}{1 + a_1 e^{-j\omega\Delta t}}$$

where Δt is the delay in equalizer feedback path, and a_1 is the relative driver strength of feedback driver against the RX differential amplifier. Δt should be about the half of the frequency that needs to be emphasized, and in our design, we used about 60ps, which corresponds to 8.3GHz. In our design, it turned out that $T_{TLINE}(\omega)$ is much less critical than $T_{AMP}(\omega)$, and that it can be ignored for design optimization. We will continue the discussion with this assumption, and will show how to optimize the equalizer only for compensating the RX amplifier performance in this paper, but the same method can be also used for compensating the interconnect loss if it is significant.

In order to optimize the equalizer and derive the optimal a_1 value, the following items need to be considered:

1. Gain peaking is the factor to determine the eye height in eye diagram.
2. Variation of group delay through RX amp. + equalizer determines the eye width in eye diagram.
3. Bit error rate is determined by the combination of the eye height and eye width.

Fig. 3 shows how the small signal AC characteristics of RX structure changes with various a_1 values. The gain and the eye height are expected to be improved with increased a_1 value. Note that the large signal amplitude of the output of the RX amplifier is limited by the VDD and Vt of devices. As a result, as shown in **Fig. 3**, as long as the rise and fall time of the input signal into RX amplifier is constant, the gain and the group delay of RX amplifier in large signal model should be almost constant from DC to 2GHz range, and the variations of the group delay no greater than 2GHz in small signal model can be ignored.

Fig. 4 shows the group delay of RX structure over 1GHz. From **Fig. 4**, it is concluded that a_1=0.2 can accomplish the least varied group delay between 2GHz and 10GHz, which is expected to achieve the best eye width and the jitter performance.

3. Silicon Measurement Results

We manufactured our proposed design on CMOS 180nm technology. Approximately 5000μm of the differential traces were implemented to achieve around 100 Ω of the differential impedance, by using the top level thick Cu metal layer. **Fig. 5** shows the photo of the test structure.

Fig. 7 shows the measured eye diagram of the output of this serial link, while **Fig. 6** shows the equivalent data on simulation, when the data rate is 8Gbps. On both of **Fig. 6** and **Fig. 7**, the eye height and eye width were improved significantly when the equalizer is activated, and it clearly indicates the effectiveness of the equalizer, and also, the simulated data and the measured data has a very strong agreement. It is concluded that our proposed design method created an optimal equalization solution.

Fig. 8 shows the measured eye diagram of the output of the serial link when the data rate is 5Gbps. The significant jitter reduction can be observed when the equalizer is on, and it indicates that the group delay of the RX structure was optimized correctly based on the proposed design method.

4. Conclusions

We implemented the on-chip high speed differential interconnect with the open drain TX driver and the self-biased RX amplifier, with the very compact equalization circuit, which should be the suitable topology for the on-chip high speed serial link of microprocessor. We

proved that our proposed design method can optimize the RX equalization circuit with ease and great performance, and finally, the design accomplished the world class performance of 8 Gbps with CMOS 180nm technology.

Acknowledgements

This work was partially supported by MEXT.KAKENHI, JSPS.KAKENHI, NEDO, and VDEC in collaboration with STARC, Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd, and TSMC.

References

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[2] R. T. Chang, et al., IEEE JSSC, Vol. 38, No. 5, pp. 834~838, May, 2003.
[3] Ron Ho, et al, IEEE JSSC, Vol. 43, No. 1, pp.52~60, Jan, 2008

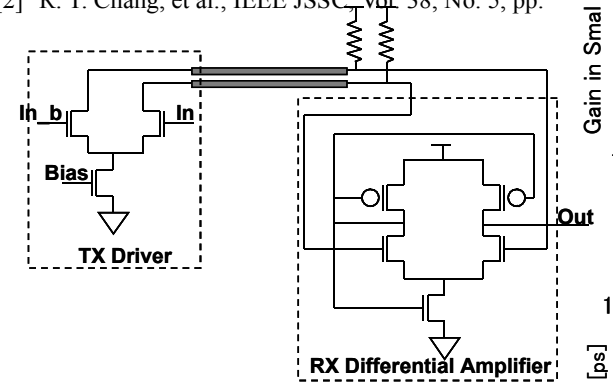

Fig. 1 On-Chip Differential Serial Link Topology

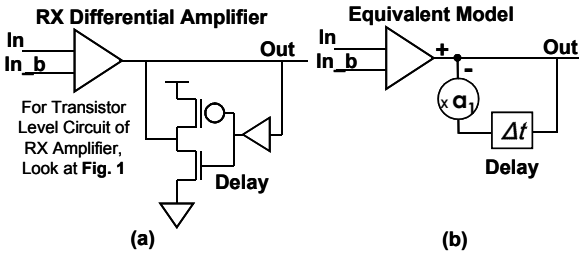

Fig. 2 (a) Equalizer Circuit, (b) Equivalent Model

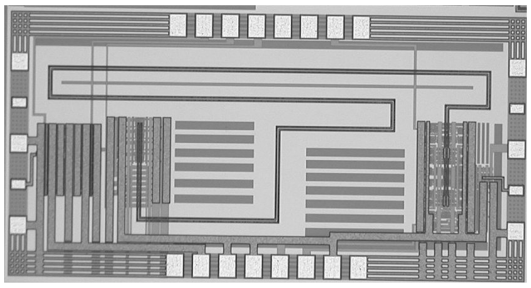

Fig. 5 Test Structure Manufactured with CMOS 180nm Technology (5000μm of differential traces)

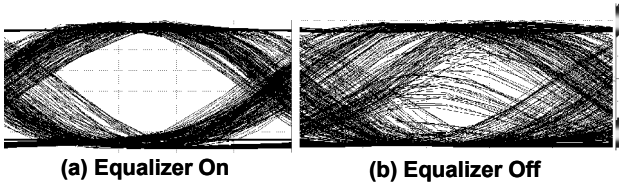

Fig. 6 Eye Diagram of Output Signal from Serial Link, (a) when Equalizer is on, (b) when equalizer is off (Simulation with CMOS 180nm, Data Rate = 8Gbps)

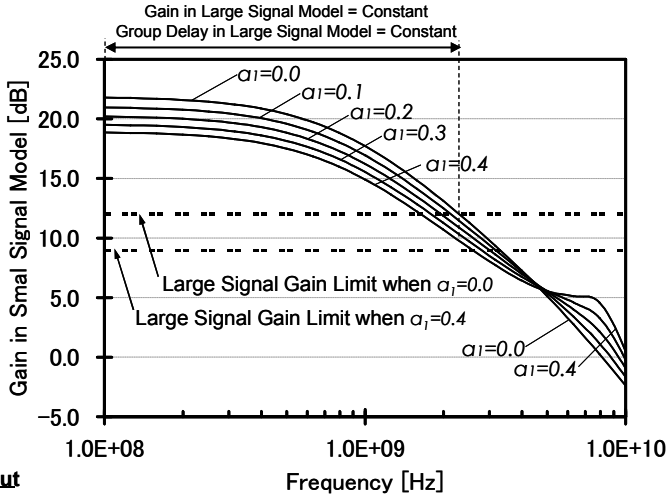

Fig. 3 AC Characteristics of RX Amplifier + Equalizer with Various a_1 Values

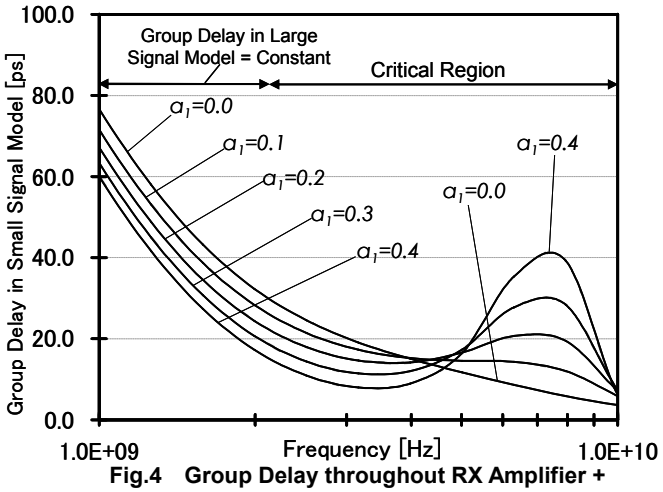

Fig.4 Group Delay throughout RX Amplifier + Equalizer with Various a_1 Values

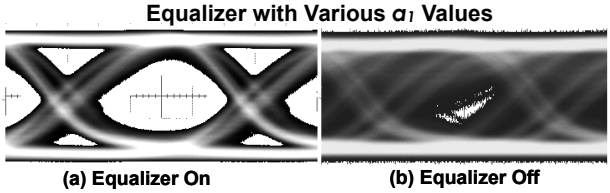

Fig. 7 Eye Diagram of Output Signal from Serial Link, (a) when Equalizer is on, (b) when equalizer is off (Measured, CMOS 180nm, Data Rate = 8Gbps)

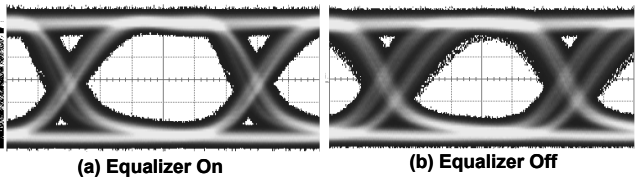

Fig. 8 Eye Diagram of Output Signal from Serial Link, (a) when Equalizer is on, (b) when equalizer is off (Measured, CMOS 180nm, Data Rate = 5Gbps)