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A Novel CMOS 800 Mb/s BPSK Detector for IR-UWB Communication

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1. Introduction

Federal Communications Commission (FCC) defined Ultra-wideband (UWB) as a spread spectrum communication system, the fractional bandwidth of which is 20 % of total bandwidth measured at -10 dB [1]. At present, three methods are being adopted for UWB implementations: direct sequence spread spectrum (DS-SS), multi-band orthogonal frequency division multiplexed (OFDM) and carrier less impulse radio UWB (IR-UWB). The IR-UWB approach, consisting of sending short duration impulses, modulated in time, polarity and amplitude, are well suited for low complexity and low power communications [2]. Gaussian monocycle pulse (GMP) is commonly used for IR-UWB systems to reduce transmission loss and to have a good matching with antenna [3]. Several detection schemes are presented in [4] - [6], which need some blocks like correlator, mixer, analog to digital converter (ADC) and so on. As a result, complexities in implementation increase. A simple CMOS detection scheme in 0.18 µm process with supply voltage of 1.8 V, capable of detecting bi-phase shift keying (BPSK) modulated differential GMP templates up to 800 Mb/s, has been presented here.

2. Architecture of the Detector

The basic functional architecture of the detector has been illustrated in Fig.1.

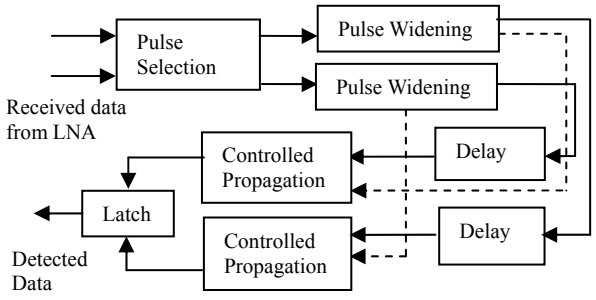

Fig. 1. Block diagram of the detector.

First, the received differential GMP templates are selected by a pulse selector to pass for further processing. The selector consists of NMOS amplifiers with active loads (MP1-ML1 and MP2-ML2), as shown in Fig.2(a). Pulses at either IP or IM will pass based on their relative phases, as shown in Fig.2(b). The pulse widening circuit in Fig.3(a), having self resetting mechanism, widens the duration of the pulses coming from the selector circuit. The pulses are widened to a span of time set by the delay of the inverter and the charging time of the capacitor, as illustrated in Fig.3(b).

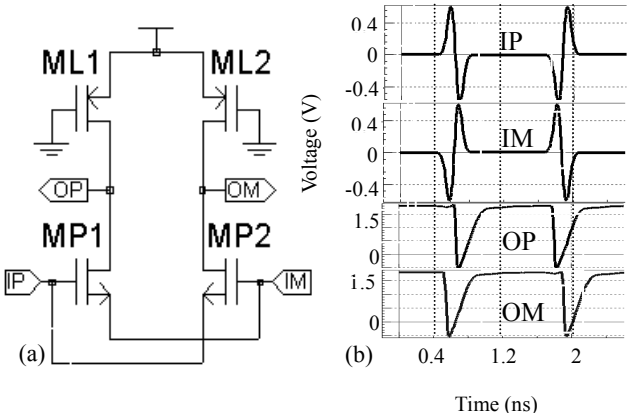

Fig. 2. The selector circuit and simulation results. (a). Schematic diagram. (b). Simulated waveforms.

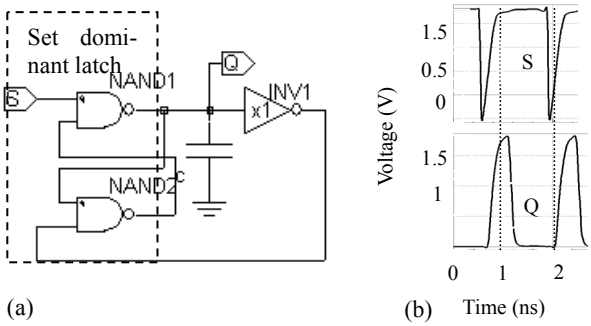

Fig. 3. The pulse widening circuit and simulation results. (a). Schematic diagram. (b). Response of the circuit.

Now, there are two widened pulses at two signal paths spaced in time at an instant, i.e. at any instant pulse at one path leads the pulse at the other path. The prolonged pulse at a path at any instant controls the propagation of the pulse

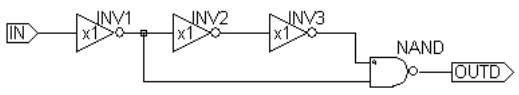

Fig.4. The delay circuit

at the other path to the latch. The pulse that comes out of the selector earlier blanks (through the block “delay”) the propagation of the other pulse to the latch. The delay, realized through some logic gates like inverter and nand shown in Fig.4 extends the input pulse duration. The overall schematic has been shown in Fig.5. The reset dominant latch is either set or reset by the propagating pulses and thus yields the detected output signals.

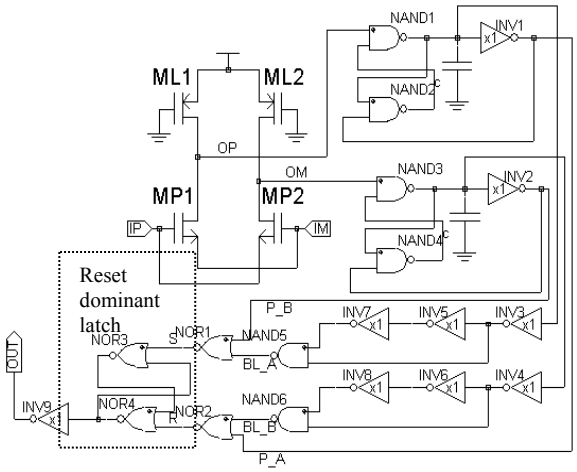

Fig.5. The overall schematic of the detector.

Here the propagation of the signal P_A is controlled by the blanking in BL_B and the signal through P_B is controlled by the blanking BL_A. Hence, if there is any blanking prior to arrival of the pulse at either P_A or P_B, it'll be stopped to pass to the latch; else it will drive the latch to generate output.Fig.6(a) and 6(b) explains the set and reset phenomena.

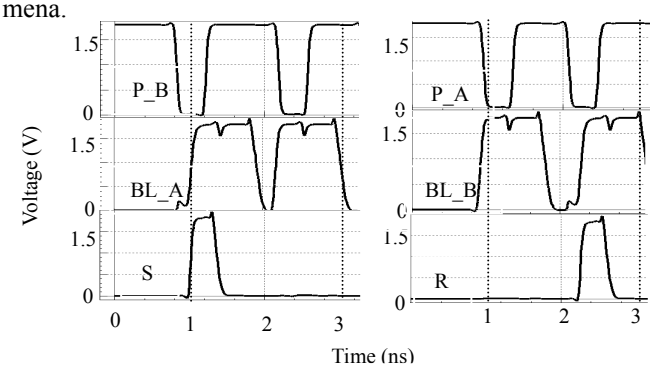

Fig.6(a). The controlled propagation mechanism. (a). Propagation through P_B. (b). Propagation through P_A.

3. Test Results

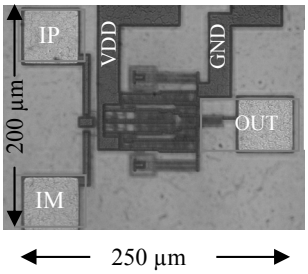

Fig.7. The chip micrograph.

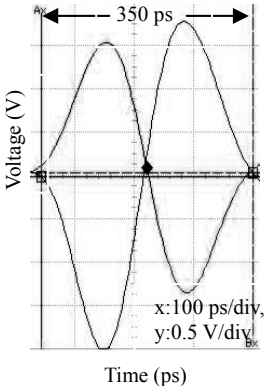

Fig.8. The input GMP.

The chip was fabricated in 0.18 µm CMOS process and the chip micrograph has been shown in Fig.7. The total area is 0.05 mm^2. The detector was tested for a random sequence of data, of 800 Mb/s, pulse width of 350 ps, modulated in BPSK scheme. The input GMP shape has been shown in Fig.8. The GMP templates modulated in BPSK, were generated by pulse pattern generator, impulse forming networks, power divider and GaAs amplifiers. The data sequence was detected successfully using a high impedance probe of transformation ratio 100:1 and the result is illustrated in Fig.9.

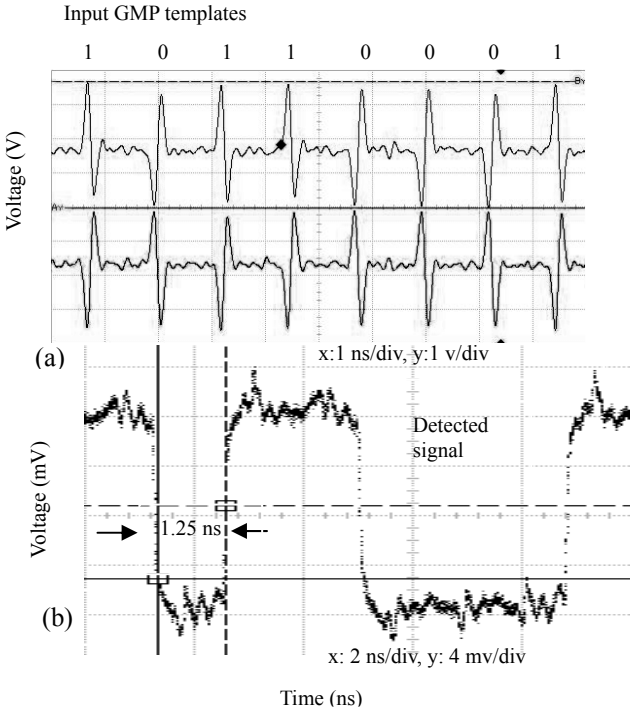

Fig. 9. The test result. (a). The input GMP templates of a random sequence of data. (b). The detected signal.

Table 1. Features of the detector

Technology	0.18 µm CMOS
Voltage	1.8 V
Modulation scheme	BPSK
Data rate	800 Mb/s
Power Consumption	4.5 mW
Die Area	0.05 mm^2

4. Conclusion

A novel detection procedure for IR-UWB is presented here. The detector, capable of detecting BPSK modulated pulse trains of data rate of 800 Mb/s, is having a die area of 0.05 mm^2 and power consumption of 4.5 mW.

References

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