Bitline-Capacitance-Insensitive Readout Circuit Using Capacitive-Feedback Charge-Integration Scheme for Low-Voltage FeRAM

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1. Introduction

Ferroelectric RAMs (FeRAM) were made practical as a small capacity non-volatile memory in the consumer products, such as a smart card [1]. In such applications, various memory sizes must be realized according to the requirements. In addition, recently, FeRAMs with scaled technology are being applied to DRAM replacement as a non-volatile cache [2]. One of the severe problems in such FeRAM technologies is a degraded stability in readout operation.

Fig. 1(a) shows conventional readout scheme for FeRAM using capacitive-division principle. Pulse voltage is applied to the plate-line PL and polarization switching charge or non-switching charge is injected to the bitline BL according to the stored information, "1" or "0." Injected charges are divided by ferroelectric capacitor CFE and bit-line capacitance C_{BL} and developed voltage is fed to a sense amplifier. For stable readout operation, the signal voltage V_{SIG}, which is defined by the readout voltage difference between stored data "1" and "0", should be as large as possible. Due to the capacitive division mechanism, however, V_{SIG} depends on C_{BL} as shown in Fig. 1(b). For small C_{BL}, sufficient voltage for polarization switching cannot be applied to the $C_{\text{FE}},$ resulting in small $V_{\text{SIG}}.$ $\;$ For large $C_{\text{BL}},$ on the other hand, V_{SIG} is simply decreases due to the decrease in the capacitance ratio $C_{FE}/(C_{FE}+C_{BL})$.

"Bitline GND Sensing (BGS) Technique," where bitline voltage is kept constant at GND level and C_{BL} -independent large readout voltage can be obtained by charge transfer mechanism of pMOS source follower, was proposed [3]. However, multiple voltage levels and complex timing control are required in this technique and therefore not suit to the small capacity memories utilized in smart card products. Furthermore, fluctuation in device characteristics cannot be compensated completely, which is becoming severe problem in low voltage operation of circuits using scaled devices.

We have newly developed a stable readout circuit for FeRAM by a capacitive-feedback charge-integration scheme using a simple CMOS inverter amplifier.

2. Proposed Readout Circuit

Figs. 2(a) and (b) show the proposed readout circuit and its operation timing diagram, respectively. The circuit is used as a preamplifier for a conventional sense amplifier. The circuit has three interesting features as follows.

(1) Capacitive Feedback Mechanism

A CMOS inverter amplifier, feedback capacitor C_F and



Fig.1 (a) Capacitive division readout circuit. (b) V_{SIG} depending on C_{BL} [3].



Fig.2 (a) Proposed readout circuit. (b) Operation timing diagram.

some switches compose a capacitive negative feedback mechanism, which forces a bitline to stay at GND level like the BGS scheme. This is the application of the well known Miller effect and works just as if an extremely large capacitance were added to the bitline. Therefore, full switching charges can be extracted and injected to the bitline regardless of small C_{BL} . Furthermore, charges injected to the bitline are integrated at C_F . Not by the capacitive division, but by the capacitive multiplication, whose ratio is C_{FE}/C_F , large output signal voltage can be obtained.

(2) Auto-Zeroing CMOS Inverter Amplifier

As a high gain amplifier composing negative feedback loop, a simple CMOS inverter amplifier is utilized. The CMOS inverter is equipped with an auto-zero mechanism which shorts input and output terminals at the reset period to compensate the threshold voltage fluctuation. This simple configuration is suited for low-voltage operation. (3) *Operating Point Shift by Charge Injection*

In the readout operation, plate-line drive causes charge injection to the bitline. Regardless of the stored informa-

tion, namely, whether for a polarization switching case or a non-switching case, however, the positive plate-line drive pulse generates positive charge injection to the bitline. Operation is, therefore, single polarity. Due to the auto-zeroing CMOS inverter operation mechanism, where reset is performed at about half V_{DD} , only about a half of the power supply rail can be utilized. The other half of the high gain operation region of the CMOS inverter is wasted. In order to enlarge the operation range and increase the output voltage swing, intentional charge injection scheme to shift the operating point was newly utilized. Synchronized with the plate-line drive pulse, negative charges are injected to the bitline through the injection capacitor C_{OS}. Appropriate amount of charge injection enlarges an available output voltage swing twice. Although attachment of C_{os} to the bitline increases the effective bitline capacitance, it is not a problem at all since the proposed readout scheme is, in principle, independent of the bitline capacitance.

3. Measured Results and Discussions

Test circuit was designed and fabricated with 0.18 µm CMOS technology. Fig. 3(a) shows a photomicrograph of the chip. Since actual ferroelectric capacitors could not be integrated, we emulated its ferroelectric characteristics with two ordinary capacitors having different capacitances as shown in Fig. 3(b). In order for setting appropriate capacitances for the capacitor emulating ferroelectric characteristics and evaluating readout signal voltages as a function of various bitline capacitances, binary-weighted capacitor array with control switches were designed for both C_{FE} and C_{BL}. Assuming typical ferroelectric thin film capacitors having a remanent polarization of 15 μ C/cm², area of 1 μ m² and plate line driving voltage of 3 V, capacitances of 144 fF and 48 fF were selected as C_{FE1} and C_{FE0} for corresponding data "1" and "0" readout. Feedback capacitor C_F and charge injection capacitor C_{OS} were designed to be 200 fF and 91 fF, respectively. Charge injection pulse voltage V_{os} was set at 3 V. Power supply voltage is also 3V.

Fig. 4 shows measured readout signal voltage V_{SIG} as a function of bitline capacitance C_{BL} . Note that C_{BL} in this graph only includes capacitance intentionally added for measurement and does not include parasitic capacitance existing essentially, which is several tens fF. Due to the available chip area limitation, C_{BL} larger than 200 fF could not be designed in this case. Different from the conventional capacitive division scheme (A), the proposed scheme (B) has no dependency on C_{BL} . Furthermore, the proposed scheme with operating point shifting technique (C) realized almost two times larger readout signal voltage than (A) and (B). It can be concluded that the proposed readout scheme can realize stable readout operation of scaled low-voltage FeRAMs.

It should be noted that the power dissipation of the proposed circuit was evaluated by simulation and revealed to be almost the same as or less than the BGS [3] scheme under the same conditions where 0.35µm CMOS technology,



Fig.3 (a) Photomicrograph of the test chip. (b) Ferroelectric capacitor emulation with ordinary capacitors.



Fig.4. Measured readout signal voltage V_{SIG} as a function of added C_{BL}

3 V power supply and 55 ns access time were assumed.

4. Conclusions

A capacitive-feedback charge-integration circuit composed of a simple inverter amplifier was applied for stable readout operation of low-voltage FeRAM. Readout signal voltage is large enough and independent of bit-line capacitance. Compared with the previous "Bitline GND Sensing" technique, configuration of the circuit and its operation are much simpler. Fluctuation of inverter amplifier characteristics can be compensated by auto-zeroing mechanism and stable operation is achieved. Charge injection scheme for increasing the signal voltage amplitude by shifting the inverter amplifier operating point was also developed.

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