Qpix, a pixel readout LSI with a built-in ADC for Particle Detector Applications

Vu Minh Khoa, Fei li, Masaya Miyahara, Takashi Kurashina and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology 2-12-1-S3-27 Ookayama, Meguro-ku, Tokyo 152-8552 Japan Tel/Fax: +81-3-5734-3764, E-mail:vuminh@ssc.pe.titech.ac.jp

1. Introduction

In recent years pixel detectors have become key components in tracking systems allowing physicist to find traces of rare particle tracks in very complicated events [1]. In gaseous ionization detectors such as GEM (Gas Electron Multiplier), if a particle has enough energy to ionize a gas, the resulting electrons emitted can cause a current flow which can be measured by readout LSI. Conventional readout pixels such as Timepix [3] can measure arrival time and time-over-threshold (TOT) which corresponds to the period of time during which the signal remained above the threshold. The deposited charge is measured via the TOT readings. However, Timepix can not provide both TOF and TOT at the same time. Moreover, TOT is affected by the slope of particle track and other factors. For example, TOT is longer for electron avalanches which come vertically than those come horizontally. Therefore to improve the detecting precision it is necessary to measure charge of particles with another method.

In this paper we introduce Qpix (Quasi-3D pixel), a pixel readout LSI for 3D particle tracking detectors which can measure charge of particles directly, via an SAR (Successive Approximation Register) ADC integrated in each pixel. TOF and TOT can also be measure simultaneously. With these excellent functions, Qpix is expected to realize detections which are a digit more accurate than that of conventional detectors. A 2x8-pixel chip was fabricated in 0.18 μ m 6-Metal 1-Poly-Si CMOS process and measured. In this paper, we describe the architecture and functional behavior of Qpix. Some preliminary experiments are also reported.

2. Pixel Structure

The pixel structure is shown in figure 1. The pixel is divided into two large blocks: the analog part formed by the preamplifier, the self-calibrating dynamic comparator, the 6-bit SAR ADC and the digital part formed by the 8-bit TOT counter, the 14-bit TOF counter, and a 14-bit register. The structure of SAR ADC is shown in Fig.3.

Any charged collected at the input pad causes a current $I_{\rm IN}$ to flow into the negative input of preamplifier. The output current $I_{\rm INT}$ is integrated at capacitance $C_{\rm s}$ and results in the output voltage $V_{\rm OUT_I}$ as follows:

$$V_{\rm OUT_I} = \frac{1}{C_{\rm S}} \int I_{\rm INT} dt$$

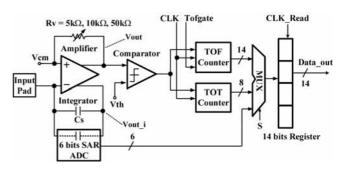


Fig. 1 Pixel structure.

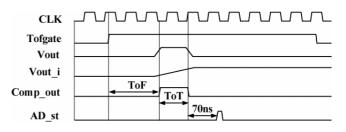


Fig. 2 Timing chart of Qpix.

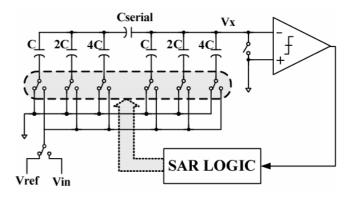


Fig. 3 Structure of SAR ADC

This voltage is sampled and converted to digital codes by the SAR ADC providing information of deposited charge. Also, I_{INT} is copied to another branch of amplifier causing a current I_{AMP} flowing into resistor R_V . This current generates the voltage V_{OUT} at node Y as follows:

$$V_{\rm OUT} = R_{\rm V} I_{\rm AMP}$$

This voltage is then compared to a threshold by the comparator. Comparator detects any signal above the

threshold. Since the gain of Opamp is quite large (100dB) we have:

$$I_{\rm IN} \approx I_{\rm INT} \approx I_{\rm AMP}$$

Clocks of the counters are synchronized with global clock CLK. TOF counter is incremented from the rising edge of Tofgate until the comparator is activated. Here, Tofgate is used as time reference. TOT counter is incremented continuously while the input signal is over threshold. The preamplifier is used as a combination of an I/V converter and an integrator. The gain of preamplifier can be controlled by the variable resistor $R_{\rm V}$. The integrating capacitor $C_{\rm S}$ is connected in parallel with the capacitor array of the ADC. By doing this we can reduce the ADC's sampling error cause by offset of preamp. The falling edge of the comparator's output is used to generate a pulse AD_st which starts A/D conversion. Data stored in counters and ADC is read out parallel through multiplexer and register. The timing chart of Qpix is shown in Fig.2. The pixel dimensions that are 140 x 200 μ m² (Fig. 4) and the static power consumption is $350 \ \mu\text{W}$ at clock frequency of 100 MHz.

3. Experimental results

Measurements were carried out using an external test pulse. Fig.5 shows the experimental results of a single pixel. Fig.5 (a), (b) show TOT and TOF measurements. The pixel can measure the TOT and TOF with an accuracy of 10ns. Fig.5 (c) shows the ADC measurement. The ADC dimensions are 70 x 200 μ m² and differential nonlinearity (DNL) is smaller than 0.25 LSB (Least significant bit). Qpix can measure an input charge up to 1.5 pC. Measurements show very good agreement with theory.

4. Conclusions

The Qpix chip has been designed using a 0.18 μ m 6-Metal 1-Poly-Si CMOS process, with a pixel cell of 140 x 200 μ m². Each pixel with a built-in SAR ADC can measure arrival time, TOT and charge simultaneously. Initial measurements verified all functions of the pixel and show very good agreement with theory. Qpix is a very hopeful tool in high-accuracy 3-D particle tracking applications.

Acknowledgements

We would like to express sincere thanks to all the contributors to the Qpix project.

References

- X. Llopart, et al., *IEEE Trans. Nucl. Sci.* NS-49 (5) (2002) 2279.
- [2] R. Ballabriga, et al., IEEE Trans. Nucl. Sci. 54 (2007) 1824.
- [3] X. Llopart, et al., Nucl. Instr. and Meth. A 581 (2007) 485.

