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A 14GHz AC-Coupled Clock Distribution Using Single LC-VCO and Distributed Phase Interpolators

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1. Introduction

The demand for high-frequency communications such as millimeter-wave [1], high-speed serial link [2] and 3D inter-chip interface [3] is increasing rapidly now. In these applications, power dissipation in clock distribution becomes more and more dominant as process scaling advances.

Until now, some clock distribution schemes using standing wave with on-chip transmission lines have been reported in [4, 5]. However, on-chip transmission lines suffer from variation in the edge roughness. Therefore, in these schemes, the performance degrades as the size of the interconnects reduces with device scaling. In future, this problem will become more and more serious. An intra-chip UWB transceiver with an on-chip antenna as reported in [6] is also not suitable for clock distribution due to large power consumption.

In this paper, we designed an AC-coupled clock distribution scheme which consists of distributed LC-VCO and phase interpolators. By employing this scheme, conventional current-mode-logic (CML) buffer becomes unnecessary. A single LC-VCO distributes clock signal to four points. The pitches of the points are 450 μm. In order to verify the operation, we designed and fabricated a test chip in 0.18 μm CMOS.

2. AC-Coupled Clock Distribution using LC-VCO and Phase-Interpolators

Figure 1 shows the concept of proposed clock distribution scheme. Left part shows the conventional buffer-based clock distribution. It employs a CML buffer which drives large capacitance and resistance of long on-chip interconnect. On the other hand, proposed AC-coupled clock distribution does not require power-hungry CML buffers and does not have to drive any capacitances. Therefore, AC-coupled clock distribution can achieve low-power operation.

Figure 2 shows the schematic of the AC-coupled clock distribution. It consists of a distributed LC-VCO and multiple phase interpolators.

A 2D mapping of the magnitude in distributed magnetic flux generated by the inductor of VCO can be seen in Fig. 3. The strength of magnetic flux is maximized at the corners. Hence, the phase interpolators are placed at positions with high magnetic flux.

3. Testchip Design and Measurement Setup

Figure 4 depicts the chip microphotograph fabricated in this research. The test chip was designed and fabricated in a 0.18 μm mixed-signal CMOS technology with thick top metal option. The area occupied by the circuit of the AC-coupled clock distribution is 0.23 mm x 1.55 mm.

For the measurement of this work, the test chips were mounted on a probe station (Cascade Microtech SUMMIT 11201B). The power and ground of the chips were supplied with DC probes. High-frequency output was delivered through AC probes and 2.3 mm coaxial cables.

4. Measurement Results

Measured total power dissipation at 14 GHz operation is 6.9 mW (4.57 mA under 1.51 V power supply). LC-VCO consumes 5.25 mW (3.48 mA under 1.51 V power supply). Four phase interpolators consume 1.65 mW (1.09 mA under 1.51 V power supply), while, the simulated power of the conventional buffer-based clock distribution with the same condition is approximately 28 mW. By using proposed ac-coupled clock distribution, power dissipation can be reduced by a factor of 4.

Operation at 14.007 GHz was confirmed as shown in Fig. 5. Due to the use of off-chip bias-tee, output power is very small. It is possible to achieve high output power when proposed circuit is fabricated on the chip since high value on-chip resistor is available. Besides, the number of turns of inductor in the phase interpolator is kept small due to the conservative design in this work. If the number of turns is increased, more power can be easily obtained. Measured phase noise is -79.06 dBc/Hz at 100 kHz offset and -101.66 dBc/Hz at 1 MHz offset when clock frequency is 12.96 GHz. Achieved performance is summarized in Table 1.

5. Conclusions

The clock distribution scheme with AC-coupling was designed and investigated for the first time. To verify the operation, test chips were designed and fabricated in 0.18 μm CMOS technology. Measured results show that power reduction can be obtained at 14 GHz clock distribution. Proposed clock distribution consumes 6.9 mW to distribute clock signal to four points whose pitches are 450 μm.

Acknowledgement

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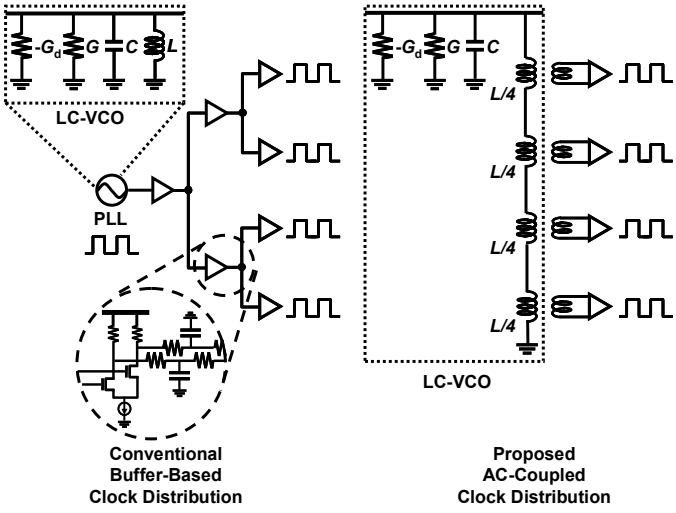

Fig. 1. Concept of this work.

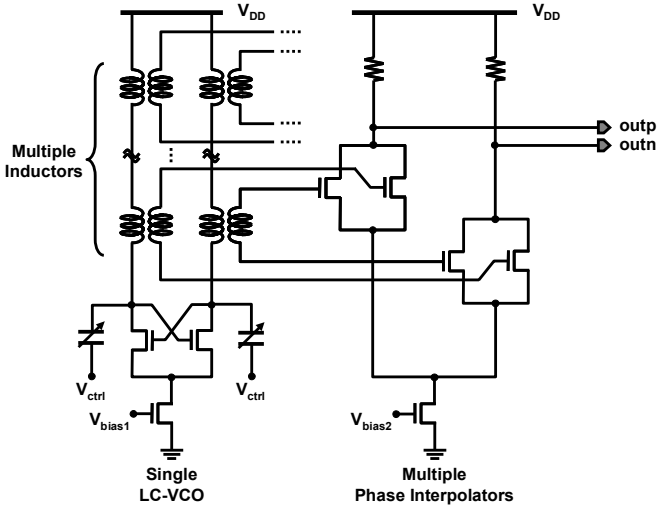

Fig. 2. Schematic of the proposed ac-coupled clock distribution.

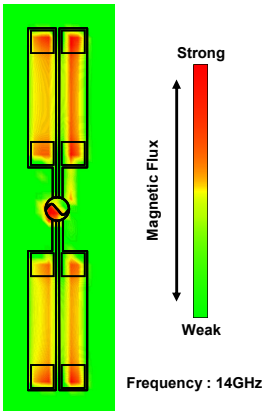

Fig. 3. 2D mapping of magnetic flux from inductor of VCO.

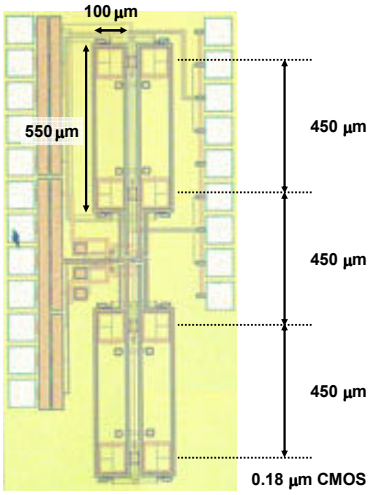

Fig. 4. Chip microphotograph.

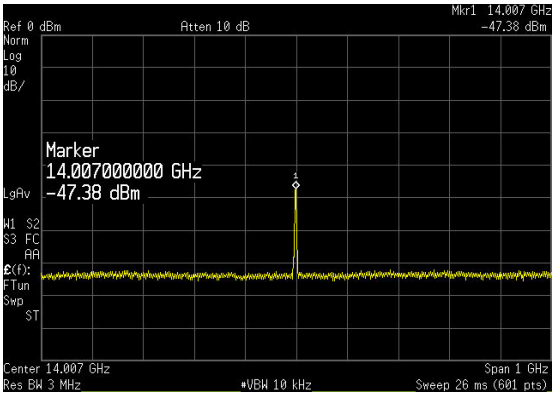

Fig. 5. Measured spectrum of output at 14 GHz.

Table. 1. Performance summary.

Process	0.18 μm mixed-signal CMOS
Power Consumption	6.9 mW { 5.25 mW (LC-VCO); 1.65 mW (4 Interpolators) }
Occupied Area	1.55 mm x 0.23 mm
Clock Frequency	14.007 GHz
Distributed Points	4 points (450 μm pitch)
Phase Noise (at 12.96 GHz)	-79.06 dBc/Hz (100 kHz offset) -101.66 dBc/Hz (1 MHz offset)