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C-6-1

Optimization of Bulk+/SON Integration for Low Stand-by Power (LstP) Applications

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Introduction

Recently, we proposed the "3D" folded Bulk+/SON structure as an innovative device allowing handling several requirements of deep scaled devices for LstP logic and SRAM application [1,2]. Indeed, this structure built on a bulk wafer by using the "Silicon On Nothing" process, allows obtaining an undoped fully depleted (FD) channel transistor with improved electrostatics and variability. In addition, thanks to the optimization of the epitaxy process, important drive current can be obtained on narrow devices, helping to enhance circuit delay when parasitic capacitance starts to be a limiting factor. In this paper, we discuss the process modules optimization of these devices in terms of V_t modulation, local BOX fabrication, Ground Plane optimization, and junction design. In addition we demonstrate the co-integration of Bulk I/O together with logic Bulk+/SON devices.

Bulk+/SON Process Flow Overview

Fig.1 describes the process flow used for device fabrication. After Shallow Trench Isolation processing and deep well implantation on a standard bulk wafer, a selective epitaxial growth (SEG) of SiGe alloy is performed, followed by a Si SEG. This latter will determine the conduction channel thickness, whereas the first will be used as a sacrificial layer to fabricate locally a buried dielectric. Si thickness (i.e. <10nm) is about $L_g/4$ in order to maintain a good electrostatic of the FD device. In this work SiGe thickness is 15nm or 30nm and will determine the buried dielectric thickness, as well as the "3D" extension of the device [2]. After gate stack patterning, the S/D regions are recessed and the remaining SiGe alloy under the gate is removed by hot HCl process [3]. Note that the Ge fraction is optimized in order to facilitate this step. The silicon channel stands above a void (giving its name to the SON technology), that is filled with ONO dielectric. Details of this step will be discussed below. Next S/D region are reconstructed using a Si SEG, followed by SD implantation, anneal and silicidation. Device morphology is shown in Fig. 2.

Process Modules Optimization

Gate Stack : For LstP applications, n+/p+ like gate electrode is not suitable for Bulk+/SON devices, since it leads to an excessively low V_{th} that requires high doping level to be increased. Therefore, the use of a mid-gap gate (in combination with a high-K dielectric to reduce the gate leakage) is preferred (Fig. 3) and allows keeping an undoped channel for high-Vt devices and SRAM devices.

V_{th} Modulation : Using Hf-based dielectric with 10nm of TiN as gate stack electrode, the undoped-channel transistor Vt (HVT) is about ~0.5V, that is well in line with LstP requirement. Nevertheless, reaching lower V_{th} (LVT) is required especially in critical path where speed in needed. Reducing the TiN thickness down to 5nm is an effective way to reach a lower nFET Vth [4] (fig. 4). On pFET side, no such effect appears, and we compensated the high-V_{th} by a BF_2 counter doping implant. As a result, LVT devices with V_{th} of 0.25V and nFET and -0.25V on pFET (Fig. 4 & 5) can be obtained while keeping a proper DIBL. A mutli-Vth platform can be achieved by co-integrating thin 5nm TiN for nFET in low V_{th} logic part, 10nm TiN in combination with counter doping for low V_{th} logic's pFET , and 10nm TiN with undoped channel for SRAM transistors (both n & p) and high V_{th} logic parts.

Ground Plane: We used two different integration schemes in order to fabricate a highly doped area under the BOX. That will be used as both anti-volumic-punchtrough and Ground Plane. In scheme A, a surfacic and high dose implant is carried out just before the SiGe/Si SEG (fig 6). In Scheme B, a halo-like implantation is performed after the gate patterning (fig. 7), and optimized in order to minimize the residual dose into the FD channel. If devices fabricated without any implants are showing volumic punchtrough, both process A and B are efficient in suppressing this leakage (fig. 8). As expected [5], the implementation of a GP leads to DIBL enhancement (especially on nFET – Fig. 9) for both scheme A and B, and also to an increase of the threshold voltage. V_{th} shift is about 90mV with scheme A for both nFET and pFET, but is found to be 140mV on nFET and 40mV on pFET with scheme B. Another difference is reflected through the matching behavior: with scheme B nFET Avt is degraded, but improved on pFET with respect to scheme A. We explain this phenomenon by the enhanced (reduced) diffusion of As-type (B-type) GP on nFET (pFET) trough the SiGe layer during the thermal treatment of gate stack.

Buried Dielectric fabrication and optimization: Detailed process steps of the buried dielectric formation are illustrated in fig. 10 . After SiGe removal, the cavity is filled first with an HTO oxide, then with a SiN. HTO oxide is used as an etch stop layer for the self aligned SiN removal by dry etch. An initial RTO step can be performed to passivate the back interface of the channel but has no effect on the device performance (Fig. 11). The SiN material optimization is critical, since the presence of fixed charge can lead to the creation of a parasitic channel at the BOX interface as shown in fig. 12, and can be responsible for an excessive source-drain leakage.

SD Optimization: At the contrary of FDSOI devices, the S/D optimization on Bulk+/SON is similar to the one of bulk transistor. Once the GP implantation is optimized, it is possible to reduce the access resistance on the nFET by increasing dose and energy of the As implantation used in deep S/D, without any degradation of the electrostatics (which is mainly controlled by the FD channel),see Fig. 13. On the pFET side, the use of C+Ge+B cocktail implant allows limiting the B diffusion, and participates to the proper control of the volumic punch-trough (Fig. 14). Note that the use of laser anneal is found to be ineffective on device performance, since it mainly reduces the poly-depletion of poly-Si gates, and does not improve Rsd (in good agreement with [6]).

Co-integration of Bulk and SON devices

Separated Bulk and Bulk+ area can be easily defined prior to the initial SEG steps. To perform this demonstration we used the thick oxide layer to prevent SiGe/Si growth SEG on I/O area. As a result, only core devices are epitaxied and transformed into Bulk+ during the SiGe etch process, leaving the I/O area as pure bulk. TEM cross section on fig. 15 shows the co-integration, while electrical performances of the co-integrated bulk devices are shown on Fig.16.

Conclusion

We described the various process optimization steps necessary to build a Bulk+ device, co-integrable with bulk transistor and usable into an LstP platform.

References

[1] F.Boeuf et al., SSDM 2005
[2] G. Bidal et al., VLSI 2008
[3] N. Loubet et al., SSDM 2008
[4] R. Singanamalla et al., EDL May 2006
[5] C. Fenouillet et al, SSDM 2008
[6] A. Cros et al, SSDM 2008

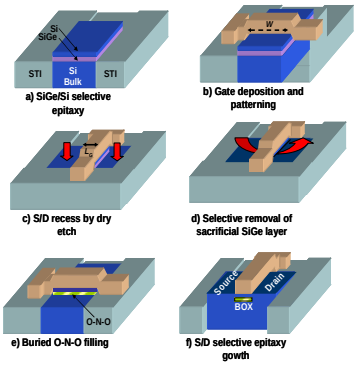

Fig. 1 : SON/Bulk+ Process Flow Scheme

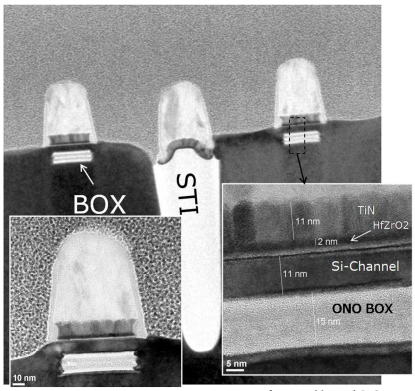

Fig. 2 : TEM pictures of Bulk+/SON device

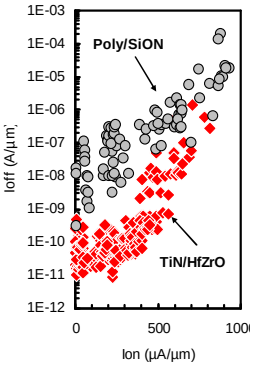

Fig. 3 : I_{on}/I_{off} trade off for Poly/SiON versus TiN/HfZrO2 gate stacks

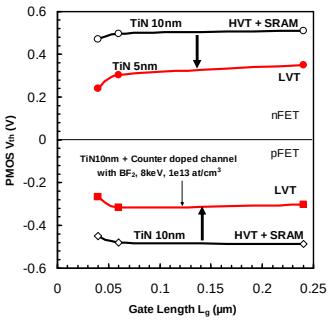

Fig. 4 : Multi-V_{th} for Bulk+/SON using WF modulation and channel counter doping

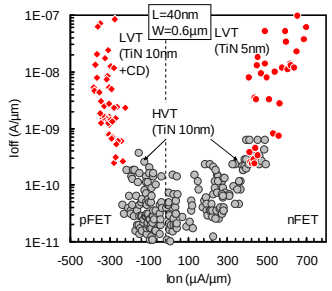

Fig. 5 : I_{on}/I_{off} trade off on multi Vth device (W=0.6µm)

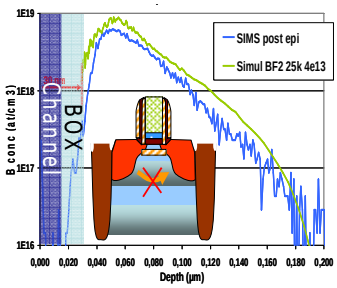

Fig. 6: Ground Plane Scheme A . Implantation is performed after Si/SiGe epitaxy

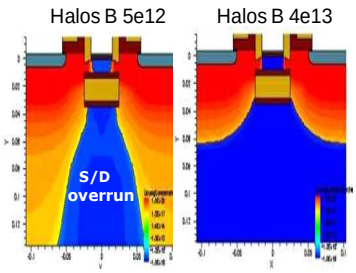

Fig. 7: Ground Plane Scheme B by optimization of post gate patterning Halo implantation .

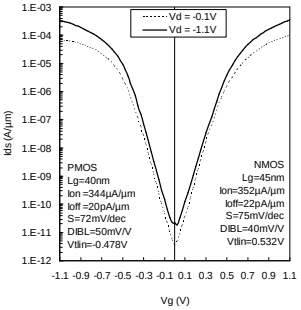

Fig. 8 : Volumic punchtrough suppression on LstP device (W=0.6µm) with Ioff = 20pA/µm

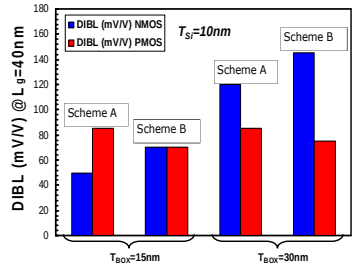

Fig. 9 : DIBL dependence on GP implantation scheme (A or B) and TBOX

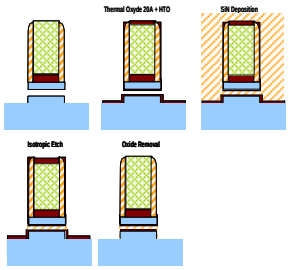

Fig. 10 : Buried Dielectric fabrication sequence

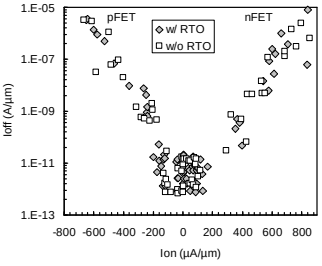

Fig. 11 : Impact of RTO anneal prior to HTO+SiN filling (W=0.6µm)

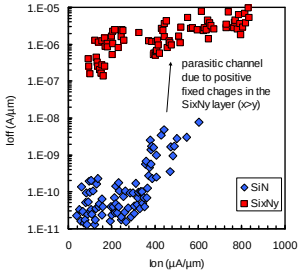

Fig. 12 : impact of SiN material on device leakage

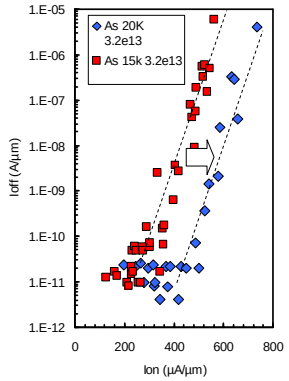

Fig. 13 : nFET S/D optimization

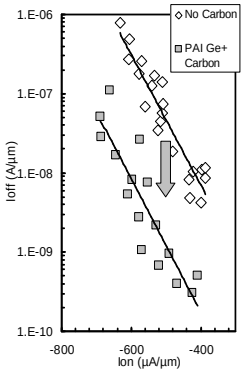

Fig. 14 : pFET S/D optimization

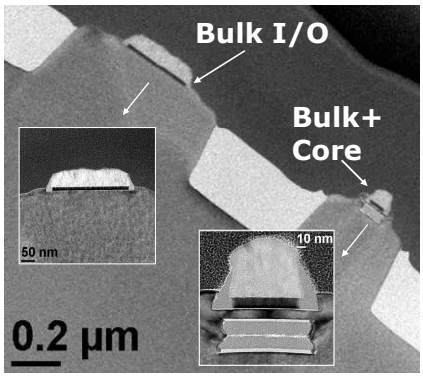

Fig. 15 : TEM picture showing co-integration of Bulk I/O and Bulk+/SON core devices on the same chip.

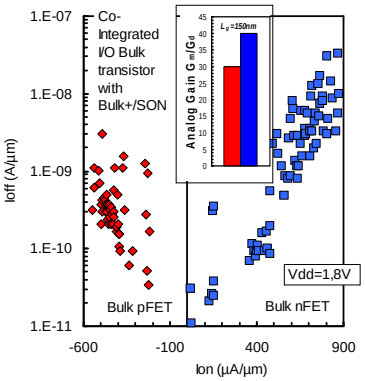

Fig. 16: I_{on}/I_{off} and Analog performance of co-integrated I/O Bulk transistors (L=0.15µm)