Sub-30 nm CMOSFET with Ni(Pt)-FUSI/SiON gate stack

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1. Introduction

Metal gate (MG) electrode is a promising technology to improve electrical characteristics and their fluctuations of planar field-effect transistors (FETs) by scaling the T_{inv} [1]. In principle, the metal gate should be compatible with a conventional fabrication procedure of the planar FET with multiple strain enhancement techniques because the channel strain should be maintained to achieve the higher drive current. From this viewpoint, the MG/SiON gate stack is more attractive than that using a high-k insulator (HK) to eliminate gate depletion for scaling the T_{inv}. This is because the better SiON/Si interface characteristics are expected to avoid degradation of the carrier mobility as reported for various MG/HK stacks [2]. In contrast, introducing the MG is considered to require aggressive shrinkage of the physical gate length for a certain circuit. For example, the gate capacitance should be reduced to improve an inverter delay because the inverter delay is proportional to a CV/I metric. In this study, we investigated the capability of gate length scaling without degradation of the drive current by using the MG/SiON gate stack.

2. Experimental

We have already reported that fabricating the fully silicided (FUSI) gate with maintaining the shallow S/D silicide enables to operate the transistor with the gate length of less than 30 nm [3]. Moreover, as shown in Fig. 1, the FUSI gate fabricated by hard-mask CMP method (HMC-FUSI) [4] makes it possible to maintain the channel strain induced by multiple process stressors because the HMC-FUSI method requires no change in the process conditions before activation anneal and after CESL formation. Pt-incorporated Ni silicide, which was suitable for silicidation of the transistor with the embedded SiGe S/D [5], was also used for the HMC-FUSI gate to keep the parasitic resistance in the S/D region. Threshold voltage (V_{th}) was controlled only by optimizing the dopant profile.

3. Results and discussion

Figure 2 shows the effect of the HMC-FUSI gate on the inversion gate capacitance of the short-channel nMOSFET with the gate width of 20 μm. It was found that the HMC-FUSI increased maximum gate capacitance by 15-20% whereas the V_{th} was slightly modulated. The T_{inv} was estimated from the maximum gate capacitance for various gate lengths to be reduced from 1.9 nm to 1.6 nm. The estimated decrease of 0.3 nm in the T_{inv} seems to be reasonable as suppression of the gate depletion.
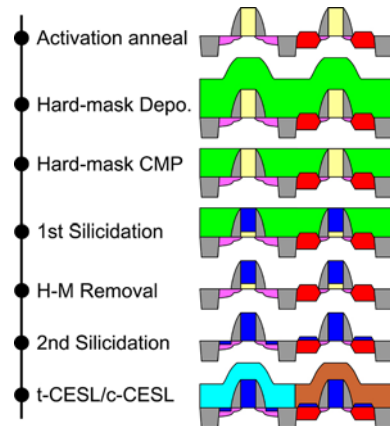

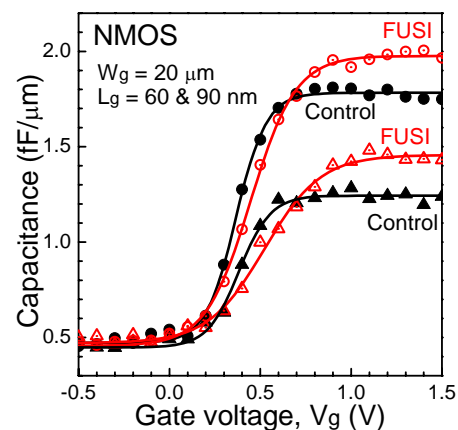Fig. 1 Key part of the process flow to fabricate the FUSI gate.

Fig. 2 V_g-C_{gc} characteristics of the n-MOSFETs
Designed gate lengths are 60 (triangles) and 90 (circles).
Black filled marks: control devices with poly-Si gates.
Red open marks: FUSI devices.

Figure 3 shows the effect of the HMC-FUSI gate on the transconductance (G_m) of the short-narrow channel n-MOSFET for low drain voltage. It was found that the HMC-FUSI gate provided the gain of 17% in the maximum G_m, which was consistent with that in the inversion gate capacitance. This result indicated that the FUSI/SiON gate stack fabricated by the HMC method caused not only no mobility degradation as observed in the MG/HK stack but also no strain enhancement induced by the melt FUSI gate [6]. Consequently, the HMC-FUSI gate stack made it possible to preserve effects of the multiple stressors used in the control devices on the electrical characteristics.

Figure 4 shows the effect of the HMC-FUSI gate on the V_{th} roll-off characteristic of the n-MOSFETs. It was found

that the HMC-FUSI made the minimum gate length of the operating transistor shrink by more than 15 nm because of the T_{inv} scaling and modulation in the effective work function of the gate.

Figure 5 plots the I_{on}-I_{off} characteristics of the HMC-FUSI n-MOSFETs corresponding to those used in Fig. 4. We achieved the drive current of 1.1 mA/μm at the off-leakage current of 50 nA/μm for the V_d of 1 V, which was much better than our previous work [3] and was competitive with that reported for the MG/HK transistor fabricated under the gate-first flow in an early stage [7].

We also achieved the drive current of 0.65 mA/μm at the off-leakage current of 50 nA/μm for the sub-30 nm HMC-FUSI p-MOSFET, as shown in Fig. 6.

Fig. 5 I_{on}-I_{off} characteristics of the FUSI n-MOSFETs. Black filled triangles: poly-Si gate devices with CMP process. Open circles: FUSI devices.
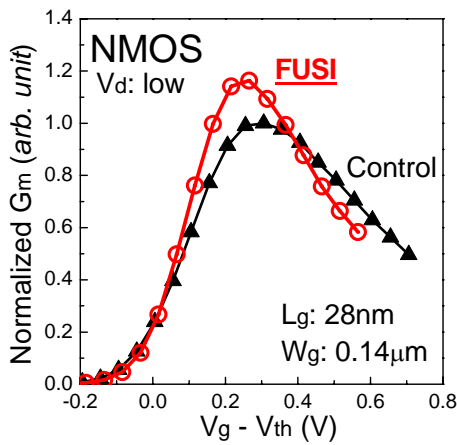

Fig. 3 Dependence of the transconductance of the short and narrow channel n-MOSFET on the gate stack
Black filled marks: control device with poly-Si gates.
Red open marks: FUSI device.
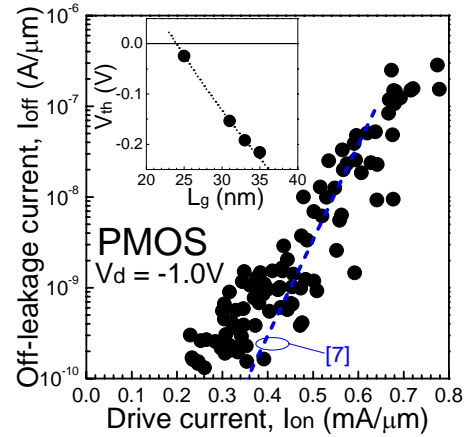
Fig. 6 I_{on}-I_{off} characteristic of the FUSI p-MOSFETs

4. Conclusions

We demonstrated an ideal T_{inv} scaling without degradation in the channel strain of the short-channel planar transistor by the Ni(Pt)-FUSI/SiON gate stack. We have achieved the drive currents of 1.1/0.65 mA/μm at the off-leakage current of 50 nA/ μm for the sub-30 nm n- and p-MOSFETs. Because shrinkage of 30% in the gate length was larger than the T_{inv} scaling of 20% with maintaining the high drive current, the FUSI/SiON gate stack would improve the intrinsic delay of the scaled inverter.
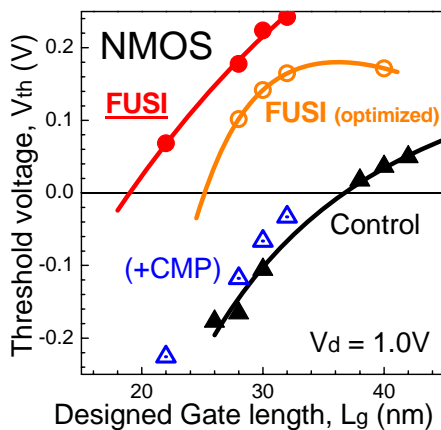

Fig. 4 Effects of FUSI formation process on the threshold voltage roll-off characteristic of the n-MOSFET.
Black filled triangles: control devices with poly-Si gates.
Blue open triangles: poly-Si gate devices with CMP process.
Red filled circles: FUSI devices. Orange open circles:
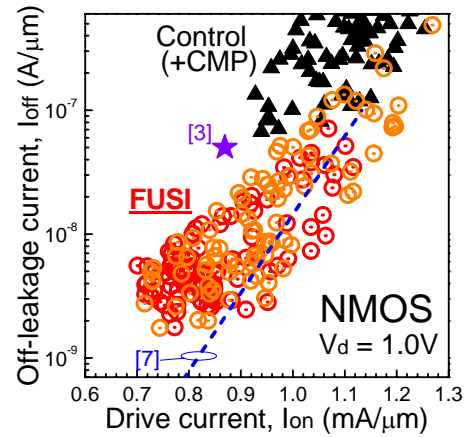FUSI devices after optimizing dopant profile

References

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