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High Performance High-K Metal-Gate Poly-Si TFTs with Subthreshold Swing < 200 mV/dec for Monolithic 3D Integrated Circuits Applications

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1. Introduction

The 3D-ICs have been believed as one of candidates for IC structures to beyond Moore's law as scaling down to reach physic limitation in the future [1]. The sequential process [2] of monolithic 3D-ICs has the advantage of low cost as compare with wafer bonding process [3]. The high performance upper transistors will be developed to compatible with base CMOSFETs, the high-K metal gate (HKMG) poly-Si TFTs could be a solution. With the experience of flat panel display, the poly-Si TFTs have the property of low temperature process to meet the requirement of monolithic 3D-ICs, which is processing after base transistors. Recently, hafnium based oxide becomes a mainstream to develop the future high-K gate-dielectric material in MOSFET due to its high-K value (~ 25), widebandgap, acceptable band alignment, and superior thermal stability [4][5]. The poly-Si TFTs with thick hafnium based oxide (> 20 nm) have been reported the subthreshold swing (SS) as 280 mv/dec [6] and 300 mV/dec [7] for n-channel and p-channel, respectively. In this work, we will integrate ultra-thin $HfSiO_x$ and TiN gate stack with TFTs for high performance applications, such as monolithic 3D-ICs, and AMOLED.

2. Devices Fabrication

The fabrication started by depositing a 300-nm amorphous Si (α-Si) layer at 550 °C by LPCVD on Si wafers capped with a 0.6-μm thick wet oxide layer. The deposited α-Si layer was then recrystallized by solid phase crystallization (SPC) process at 600 °C in a N_2 ambient. The grain size and roughness of 300-nm poly-Si with SPC crystallization are 100 - 150 nm and ~ 3 nm by AFM (Fig. 1), respectively. Then, after removing the native oxide by dipping in diluted HF solution, an ultra-thin $HfSiO_x$ and 200-nm TiN was deposited in a MOCVD at 550 °C and sputtering system at RT, respectively. The gate stack was defined by lithograph and etching process. Next, a self-aligned As ion implantation was performed at 25 keV to a dose of 5×10^{15} cm^{-2} to dope source/drain region (Fig. 2). The annealing process for dopant activation was performed by RTA in an N_2 ambient with 2 steps. The step 1 is 600 °C for 100 sec, and step 2 is 650 °C or 700 °C for 10 sec. The bulk Si was also fabricated with the same process flow for control sample.

3. Results and discussions

After all thermal budget of process, the physical thickness of $HfSiO_x$ and interfacial layer (IL) by cross sectional HRTEM are 3.0 and 1.5 nm, respectively (Fig. 3), the poly grain boundary (GB) can be also observed. The equivalent-oxide thickness (EOT) and the effective dielectric constant of $HfSiO_x$ are extracted by bulk Si C-V characteristics (Fig. 4) to be 2.8 nm and 9, respectively. The transfer characteristics of HKMG poly-Si TFT with 700 °C annealing shows on/off ratio > 10^6, and the SS can achieve 193 mV/dec for L_g = 0.3μm of 700°C devices at room temperature operation (Fig. 5). The output characteristics exhibits the high driving current and indicates the effective mobility μ_{eff} = 33 cm^2/Vs (Fig. 6). The parasitic effect by S/D resistance of 700 °C devices has improved 10x as compare with that of 650 °C, and leads to diminish short channel effect as devices scaling down (Fig. 7). The short channel effect by observing V_t will occur with L_g < 1 μm. However, the DIBL has reverse behavior as L_g < 0.5 μm due to the grain size is ~ 0.3 μm and less GBs for short channel devices. For reliability of both hot carrier and PBTI, the short channel devices show more stable in V_t than that of long channel devices (Fig. 8). Much GBs have to cross while the electrons transport from source to drain for long channel devices and was also proved by DOS extraction (Fig. 9). The traps scattering by GBs and phonon scattering will be decreased at low temperature (LT) operation, and it makes the I_D leakage significant decreasing (Fig. 10). The V_t linearly decreases with temperature with a slope of -1.6 mV/K (Fig. 11). This excellent value is close to the value obtained in bulk Si devices (~ -2 mV/K) [8]. As expected, the SS linearly decreases with temperature with a slope of -0.77 $mVdec^{-1}K^{-1}$.

4. Conclusions

We have successful demonstrated high performance HKMG poly-Si TFTs with SS = 193 mV/dec for L_g = 0.3 μm. The highest thermal budget is 700°C, and it is compatible with monolithic 3D-ICs process. The short channel devices exhibit better reliability as compare with long channel devices due to less GBs. We proposed the HKMG poly-Si TFT be a candidate to pave a way for future monolithic 3D-ICs applications.

5. Acknowledgements

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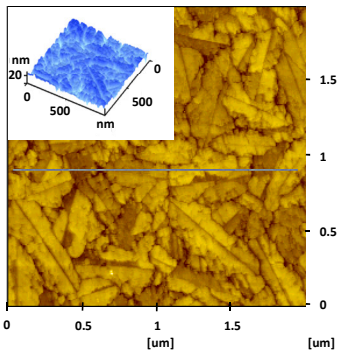

Fig. 1. The surface morphology of poly-Si with SPC crystallization by AFM. The thickness is 300 nm. The grain size and roughness are 100 - 150 nm and ~ 3 nm, respectively. The inset shows the 3D surface morphology.

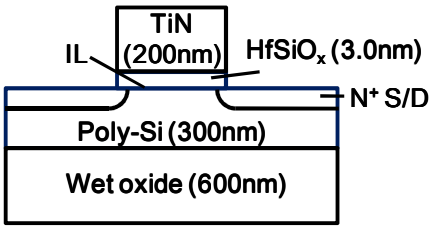

Fig. 2. The schematic diagram of HKMG poly-Si TFT. The one-mask process was used to fabricate HKMG poly-Si TFTs.

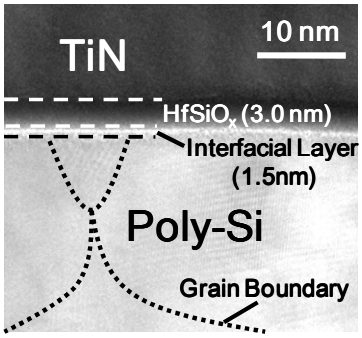

Fig. 3. The cross section HRTEM of HKMG poly-Si TFT. The interfacial layer was observed after all devices fabrication process.

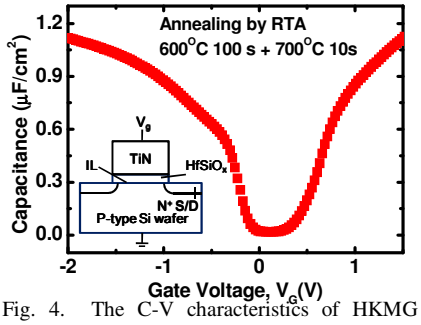

Fig. 4. The C-V characteristics of HKMG on bulk-Si. It was also fabricated with the same process flow, and the highest thermal budget is 700°C.

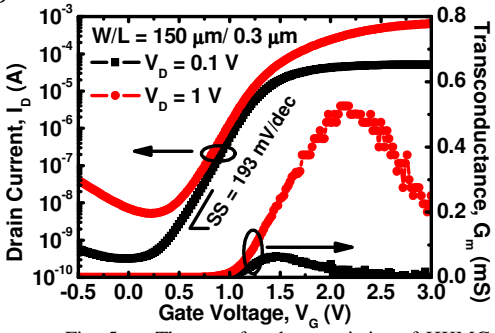

Fig. 5. The transfer characteristics of HKMG poly-Si TFT with 700°C annealing. The on/off ratio is > 10^6, and SS is 193 mV/dec for device W/L = 150 μm/ 0.3 μm.

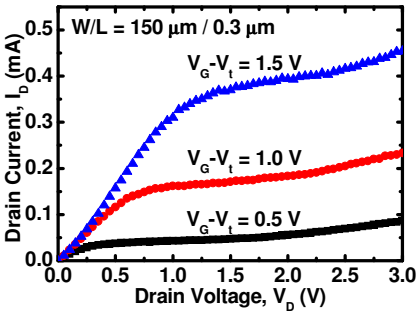

Fig. 6. The output characteristics of HKMG poly-Si TFT with 700°C annealing. It exhibits the high driving current and indicates the effective mobility μ_{eff} = 33 cm^2/Vs.

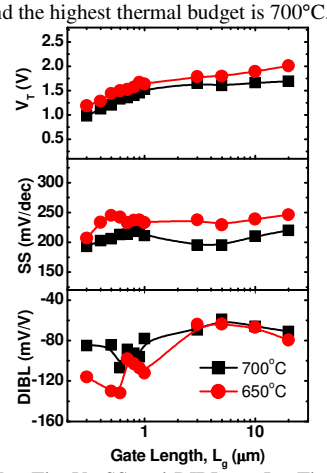

Fig. 7. The V_t, SS and DIBL vs. L_g. The parasitic by S/D resistance of 700 °C devices has improved 10x as compare with that of 650 °C.

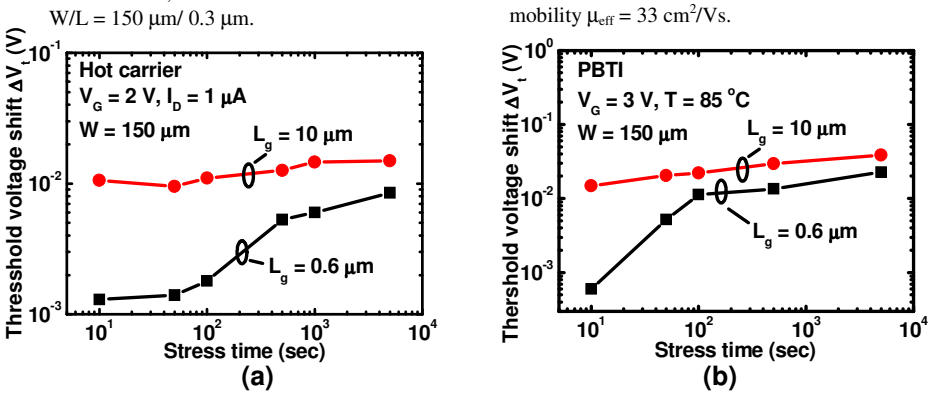

Fig. 8. The reliability of HKMG poly-Si TFTs for (a) hot carrier, (b) positive bias temperature instability (PBTI). The short channel devices show more stable in V_t than that of long channel devices due to less GBs from source to drain.

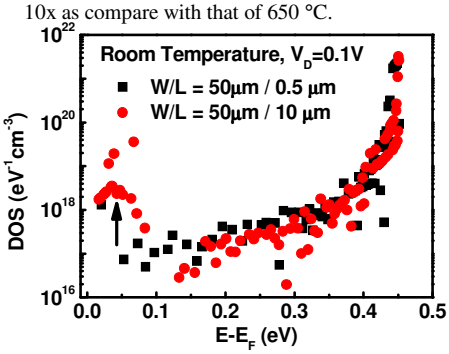

Fig. 9. The extracted DOS of HKMG poly-Si TFT. The higher trap state was obtained for long channel devices indicates the much GBs to cross as carrier transportation.

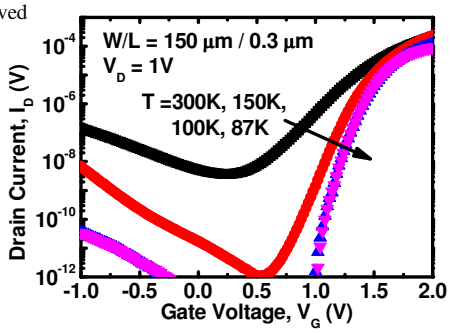

Fig. 10. The transfer characteristics of HKMG poly-Si TFT during low temperature operation. The traps scattering by GBs and phonon scattering will be decreased at LT operation, and it makes the I_D leakage significant decreasing.

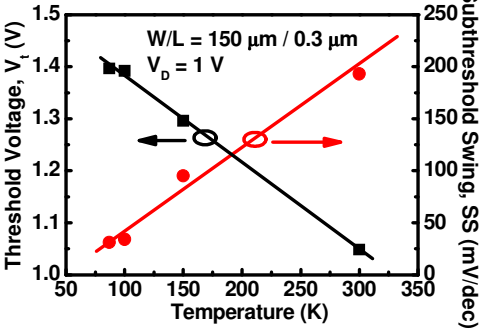

Fig. 11. The Vt and SS vs. temperature. The V_t & SS linearly decreases with temperature with a slope of -1.6 mV/K & -0.77 $mVdec^{-1}K^{-1}$, respectively.