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Separation of Interface and Bulk traps in Advanced High-k Gate Dielectric MOSFETs from a Low-Leakage Charge Pumping Technique

E. R. Hsieh[1], Y. H. Chu[1], G. D. Lee[1], S. S. Chung[1], W. M. Lin[2], C. W. Yang[2], Y. S. Hsieh[2], L. W. Cheng[2], C. T. Tsai[2], and G. H. Ma[2]
[1]*Department of Electronic Engineering, National Chiao Tung University, Taiwan* [2]*UMC, Central R&D Division, Hsinchu, Taiwan*

Abstract- A novel technique to profile the spatial distribution of interface and bulk traps in high-k gated MOSFETs from a low leakage charge pumping technique, has been demonstrated in nMOSFETs with high-k gate dielectric. Both **interface traps** (fast traps) and **bulk traps** (slow traps) show their respective impact on the device reliability. The spatial distribution of interface traps and high-k bulk traps in two dimensions can be separated. Applications to the understanding of the mechanisms in interface/bulk traps generation after PBTI stress have also been addressed.

Introduction- High-k has aroused more interests in research to extend the scaling limit of CMOS devices. It is well known that high-k has an inherent V_T instability caused by the traps at the interface between interfacial layer (IL) and Si and bulk traps in high-k layers [1]. These traps will cause electrons trapping and de-trapping, inducing gate-reliability issues, such as breakdown and V_T instability etc. Reported results have provided how to identify these traps [2-3]. In [1-3], it was described how to verify these traps by the charge pumping measurement but was not suitable for the characterization of these traps in the high-k gate dielectric. Further effort is needed for a full characterization of these traps (e.g., the separation of interface and bulk traps) and its correlation to the device reliability.

In this paper, a new method based on an earlier IFCP [4-5] which we developed, has been extended for more applications in high-k measurements. Results have been demonstrated for devices with HfSiON gated nano-CMOS devices. The spatial distribution of interface and high-k bulk traps and the correlation to device reliability has been demonstrated.

I. Device Preparation

The devices were fabricated based on 90nm CMOS technology. High-k HfSiON film was deposited by ALD and with post-NH_3 annealing. An interfacial layer (SION) was formed prior to high-k deposition. Two different implanted halos were used for studying the reliability of these devices. Halo-2 has a lighter AMU than halo(1), as shown in Fig.1. The tested devices have EOT= 10.2 Å with masked width/length = 10μm/0.09μm.

II. Results and Discussion

A. IFCP: A low leakage charge pumping technique

With reducing gate oxide thickness, I_G increases, and thus CP current will include extra I_G component. A low leakage IFCP (*Incremental Frequency Charge Pumping*) measurement [4-5] has been applied in ultra-thin oxide(EOT<20A^0) to reduce I_G leakage. Fig. 2 shows the schematic of IFCP. From the measured I_{CP} with two frequencies, we take the difference of I_{CP} currents of these two frequencies as the I_{CP} at their difference frequency since I_{CP} is proportional to *f*, in which the leakage current can be removed.

B. Characteristics of bulk(slow) and interface(fast) traps

As illustrated in Fig. 3, the steps to separate the bulk trap, $N_{bt,}$ from N_{it}, are as the following:

1. At a specified frequency, 100kHz as an example, we first take measurement for $I_{CP,5.1MHz}$ and $I_{CP,5MHz}$. Then, we subtract these two $I_{CP's}$. The net Icp can be considered to be the contribution from N_{it} only.
2. In Fig. 3, we choose two close frequencies corresponding to a position close to x, in the high-k. We measure $I_{CP's}$ for these 2 frequencies, which are subtracted with I_{CP} in step 1. The net I_{CP} becomes the contribution from N_{bt} only.
3. Followed by taking the difference of $I_{CP's}$ at the above 2 frequencies, in which the DC leakage can be eliminated.
4. Based on the trapping formula in Fig. 3, the depth profile of N_{bt} inside the high-k can be determined.

Fig. 4 shows the I_{CP} results for a control oxide (SION) and high-k gate dielectric devices. The I_{CP} is proportional for 500kHz, 1Mz, 2MHz measurements (left figure), while there is a loss of the linearity for high-k device(right figure). This nonlinearity is attributed to the bulk (slow) traps in high-k. Further shown in Fig. 5, at high frequency, interface trap, N_{it}, (fast trap) contributes to the I_{CP}, while at low frequency, bulk trap, N_{bt}, (slow trap) is dominant of I_{CP}. The bulk trap will respond to low frequency such that trapping occurs with a longer time. Based on this feature, bulk trap distribution in the high-k can be determined by varying the frequency of the CP measurement. Results are shown in Fig. 6, with N_{bt} distribution away from the high-k/SION interface.

C. Applications to the reliability and PBTI studies

To explore further merits, various reliability and PBTI induced degradations were studied. By applying the above technique, the generated N_{it} and N_{bt} after the gate bias and PBTI stress were evaluated. The results of N_{bt} distribution for two different bias stress conditions are shown in Fig. 7 and Fig. 8 respectively. Note that a negative stress induces the damage in the region near gate side, while the positive stress induces the damage in the region near substrate side. Fig. 9 shows the comparison of two stress effects for two splits, (a) and (b), respectively as a function of time. It can be seen that, for $V_G < 0$ stress, the bulk trap is not obvious, while we see a large increase of bulk trap during the $V_G > 0$ stress. Fig. 10 shows the interface trap generation for two splits, (a) and (b), respectively as a function of stress time. We can see that the N_{it} generation is larger during **gate injection**. PBTI results are shown in Fig. 11. Here, we see much larger $N_{bt's}$ were generated for halo-1 sample since this sample has larger amount of traps with a heavy implant. Also, it induces a larger N_{bt} after PBTI stress. This can be verified from the three peaks of Gated-diode measurements [6] as shown in Fig. 12. All these results can be explained from Figs. 13 (a) and (b) and summarized in Table 1. In other words, during gate injection, high energetic electrons arrive at the anode and hole leads to interface generation. However, during substrate injection, the electrons are attracted toward the high-k dielectric and give rise to an injury of the gate dielectric.

In summary, IFCP measurement method, equipped with the trap separation technique, has been able to find a two-dimensional spatial distribution of bulk (slow) and interface (fast) traps in high-k dielectric MOSFTEs. Both interface and bulk trap can be separated based on this technique. Applications to the understanding of interface/bulk traps generation after PBTI stress have been demonstrated. In particular, the depth profiling of N_{bt} in the high-k is an essential tool to understand the high-k quality of nanoscale CMOS devices.

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References

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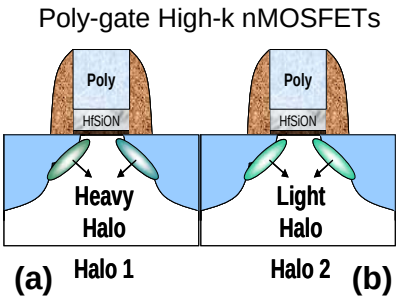


Fig. 1 Device splits prepared in this work. (a) Poly Gate high-k nMOSFETs with heavy Halo, Halo1; (b) with light Halo, Halo2.

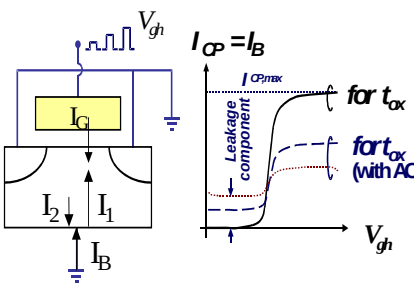


Fig. 2 (a) The schematic of charge pumping (CP) for nMOSFET measurement. (b) Leakage current occurs when t_{ox} < 20A

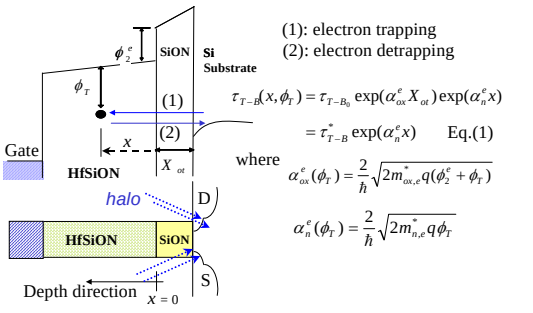


Fig. 3 Energy band diagram showing the trapping of electrons, process (1). The trap location x is measured from the high-k/interfacial layer interface. The correlation between the CP signal frequency, trapping time, τ_{T-B}, and the formula, Eq. (1) as shown, can determine the value of bulk traps, N_{ot}, at a location x, in responding to a low frequency.

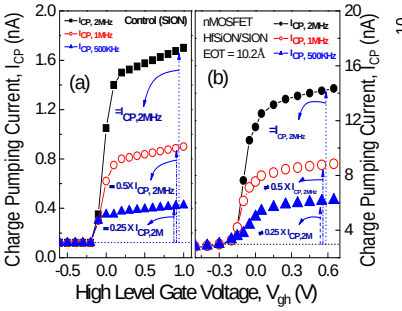


Fig. 4 I_{CP} currents for (a) control sample (SION oxide) and (b) HfSiON /SION gate stack nMOSFET devices. Note the difference in that I_{CP} is not proportional to frequency for high-k in (b).

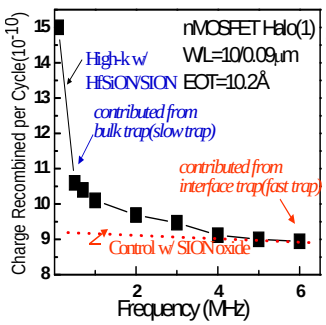


Fig. 5 Measured charge per cycle, Q= Icp/f, as a function of frequency. High-k sample exhibits a bulk-trap in high-k material, which responds at low frequency. While, control oxide sample shows a flat curve which is independent of frequency (only interface trap is dominant).

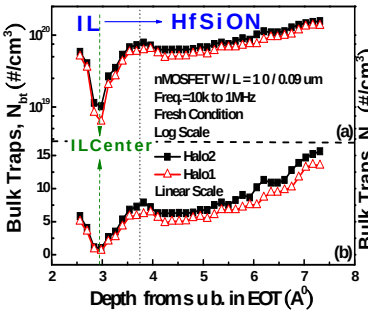


Fig. 6 Calculated spatial distribution of bulk traps in HfSiON for two different halo implants. Halo (2) has heavier AMU than halo(1), which induces more traps in the high-k bulk.

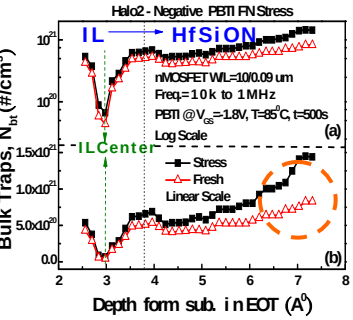


Fig. 7 Bulk trap distribution of HfSiON before and after the **negative** bias stress. Note that the region near the poly gate is damaged during negative stress.

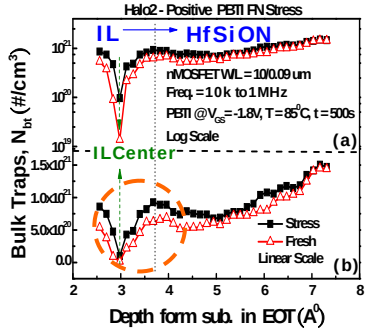


Fig. 8 Bulk trap distribution of HfSiON before and after the **positive** gate bias stress. Note that much larger traps have been created near the region near the substrate during positive bias stress .

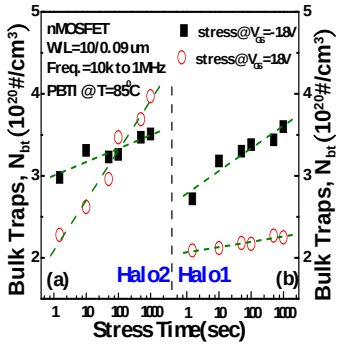


Fig. 9 Bulk trap generation as a function of stress time. It shows a much larger generation rate for **positive** gate bias stress.

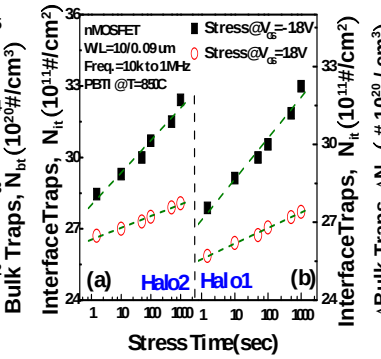


Fig. 10 Trap generation as a function of stress time, in which negative gate bias stress shows larger N_{it} generation than positive gate bias does.

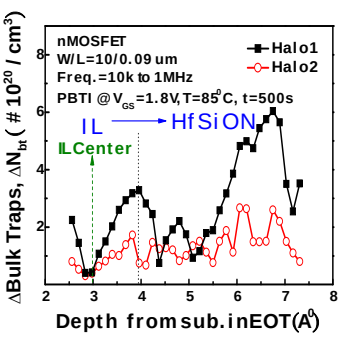


Fig. 11 Calculated N_{it} and N_{ot} distributions after PBTI stress. Note that larger N_{ot} was generated for halo(1).

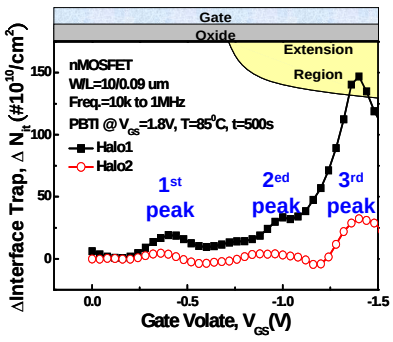
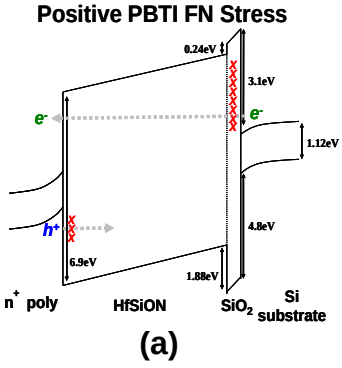


Fig. 12 Comparison of the gated-diode currents for different halo implants, in which the smaller damage in the channel and drain regions are caused by a larger initial bulk traps in halo(2).



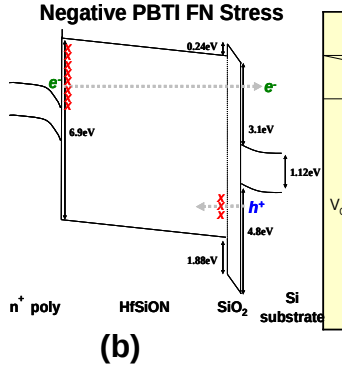


Fig. 13 (a) Band diagram of HfSiON/SION during gate injection. (b) Band diagram of HfSiON/SION during substrate injection which generates bulk trap in high-k.

HK nMOSFETs			
Reliability \ Split		Halo1	Halo2
PBTI@ V_{GS}=|1.8|V,T =85^{0}C, t=500s	Bulk Trap, ΔN_{bt}(#10^{20}/cm^3)	6.04	2.64
	Interface Trap, ΔN_{it}(#10^9/cm^2)	147	32
	Positive FN	Damage on the bottom interface b/w IL & Si	
	Negative FN	Damage on the top interface b/w Poly & HK	

Table 1 Halo-2 device is more reliable than Halo-1. Positive and negative PBTI FN stress induce damage in different parts of the bulk dielectric.