Characteristics and Integration Challenges of FinFET-based Devices for (Sub-)22nm Technology Nodes Circuit Applications

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Abstract

FinFET-based multi-gate (MuGFET) devices are considered one of the most promising device architecture candidates for enabling continued CMOS scaling beyond the 32nm technology node. They offer improved electrostatics and steeper sub-threshold slopes, with reduced $V_T$ variability due to low channel dopants concentration. This work provides an overview of FinFETs latest developments, addressing some of their main challenges and opportunities: 1) device fabrication options; 2) channel mobility enhancement; 3) mismatch behavior, showing excellent 6T-SRAM scalability.

Introduction

For the past decades, introduction of several technology innovations over different nodes has allowed keeping a rapid pace of improvement, as expressed by Moore’s law (Fig.1). With scaling of planar bulk approaching its limits, transition to non-classical device architectures is currently expected to occur after the 32nm node, though not at the same time for all applications and all chip manufacturers, because of involved costs and compatibility with circuit design [1]. In this context, FinFET appears as a particularly attractive technology since it can be implemented on both bulk-Si and SOI substrates (see Figs.2,3) [2-8], with particularly attractive technology since it can be implemented on both bulk-Si and SOI substrates (see Figs.2,3) [2-8], with functional FinFET SRAMs fabricated with planar FinFET peripheral circuits on the same bulk-Si substrate demonstrated in Ref[9].

Device Characteristics and Technology Challenges

With scaling, it is critically important to maintain/improve the channel mobility, currently enhanced by applying strain to the channel. In MuGFETs, typically fabricated on (100)/<110> vertical sidewalls channel. In MuGFETs, typically fabricated on (100)/<110> vertical sidewalls, Fins are defined to have (110)/<110> sidewall surfaces on the carrier mobility becomes predominant, affecting electrons and holes differently [10]. This can be verified in Fig.4, where only a minimal degradation is observed in the high-field electron mobility for (110) dominated FinFETs vs. planar (100) devices. For PMOS, on the other hand, as hole mobility is affected differently [10], substantially improved for the (110) transport plane, higher values are obtained in narrower Fin devices [3]. Ultimately, to be able to meet the stringent drive requirements of the ITRS roadmap, strain engineering will be needed. As for planar bulk, several strain or mobility enhancement techniques can be used for this purpose [2, 11-13], though the strain induced by most current process-induced strain techniques (e.g., use of Contact-Etch-Stop-Layers with high intrinsic stress) tends to decrease with scaling, posing an additional challenge. Fig.5 shows the results obtained upon integration of a compressively strained SiGe layer in the S/D of a p-type MuGFET, owing the 25%-performance improvement to the combined effect of improved hole mobility and $R_{DS}$ reduction [11].

Due to full depletion of the Fins, $V_T$ tuning options for narrow Fins are limited to workfunction (WF) tuning with metal gate (MG) electrode. Setting it to its desired value is an important challenge even if, when compared with planar bulk devices, FinFETs need smaller WF shifts from mid-gap to reach low or high-$V_T$ targets (Fig.6). Medium-$V_T$ values are set by a mid-gap WD electrode such as TiN deposited by PECVD. An overview of the results obtained with capping technology in MuGFETs is shown in Fig.7, with: 1) La$_2$O$_3$-cap by ALD or Dy$_2$O$_3$-cap by AVD used for low-$V_T$ NMOS (or high-$V_T$ PMOS), and 2) Al$_2$O$_3$-cap by ALD used for low-$V_T$ PMOS (or high-$V_T$ NMOS). Capping layers can be selectively inserted in the flow, either immediately after the host dielectric (HfSiO) deposition or in-between 2 TiN metal layers deposition to allow extra flexibility in the integration scheme. Capping multiple-$V_T$ CMOS on the same wafer. For the last capped gate stack configuration, cap diffusion towards the interface with the gate dielectric occurs with a high enough thermal budget (e.g., 1050ºC spike anneal), resulting in comparable (or even slightly higher) WF shifts with reduced CET and without impacting $I_D$, improved mobility, similar noise response and improved reliability behavior [14].

Despite their excellent intrinsic behavior, there is some concern that the higher parasitics of FinFETs could be a show-stopper for their introduction into production. The quest for solutions to minimize this issue is therefore critical. Fig.8 shows an increase of the series resistance $R_{DS}$ for narrower Fin devices, more strongly so for NMOS than for PMOS. This leads to drive current degradation, compromising high-speed operation. Correlating $R_{DS}$ values with $I_D$ and Fin morphology showed a clear impact of the amount of the Fin that is amorphized by the implanted species. Problematic recrystallization during junction anneal results in defect formation and poor dopant activation [15,16], with As-implanted narrow Fins (NMOS) more affected than BF$_2$- or implanted Fins (PMOS). Results for differently As-doped Fins undergoing different thermal treatments are shown in Fig.9, promoting the use of less-amorphizing, low-energy extension I/D to obtain improved Fin morphology and reduced $R_{DS}$. The implant conditions can also impact the quality and growth rate of Si-Epitaxial-Growth (SEG) for raised S/D, a well-known method to help reduce $R_{DS}$. This is shown in Fig.10, where stacking faults in the SEG are observed for strongly amorphizing I/D conditions after junction anneal, being an additional source of variability. $R_{DS}$ can also be reduced by layout optimization [17], with Ref.[18] showing limited penalty of FinFETs vs. planar devices for additional parasitics capacitance.

Circuit performance

Ever-increasing transistor variation and mismatch reduce the read stability and write margin of the 6T-SRAM cell, putting at risk its scaling viability beyond the 32/22nm nodes. With their lightly doped channels, FinFETs can avoid the stochastic dopant fluctuation issues of planar bulk CMOS, key for prolonging SRAM scaling. Sources of variability in narrow FinFETs that can be further improved are $L_{min}$, $L_{opt}$, $R_{DS}$, $R_{on}$, $R_{off}$ and $R_{on}R_{off}$ fluctuations, mentioned above. Fig.12 confirms the excellent $V_T$-mismatch behavior of undoped vs. doped FinFETs (SOI vs. bulk) and, more so, $V_T$ vs. planar bulk devices. In addition, as shown in Fig.13, they also show competitive RO performance [18]. Fig.14 shows good $\sigma(V_D)$ for the transistors of a 0.18/µm² 6T-SRAM cell, with the corresponding butterly-curves shown in Fig.15 [8].

Conclusions

In this paper, we reviewed FinFETs latest developments and covered some of their main technology challenges and opportunities for enabling continued CMOS scaling for sub-32nm nodes, with their excellent intrinsic characteristics making them particularly attractive for dense applications such as the 6T-SRAM.

References

Initial Fin

Crystalline Si performance for SOI-FinFETs. 

PMOS MuGFET devices. $R_{\text{SD}}$ was extracted by extrapolating to $L_{\text{gate}}=0$ and $|V_{\text{GS}}|=3\text{V}$ and $|V_{\text{DS}}|=50\text{mV}$.

the total resistance $R$ measured at excellent VT-mismatch.

Fig.12 – Pelgrum plot showing the excellent $V_{\text{th}}$-mismatch vs area scaling performance for SOI-FinFETs ($AV_{\text{th}}=2\text{mV \cdot \mu m}$) vs. bulk technology.

Fig.13 – FinFET Ring Oscillators show competitive Power/Speed trade-off performance ($V_{\text{th}}=4\text{V}$), when compared with planar devices.