Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp1042-1043

High-Performance three-terminal FinFETs by Combination of Damage-Free Neutral-Beam Etching and Neutral-Beam Oxidation Technologies

Keisuke Sano [1], Masahiro yonemoto[1], Akira Wada[1], Kazuhiko Endo[2], Takashi Matsukawa[2], Meishoku Masahara[2] and Seiji Samukawa[1]

[1]Institute of Fluid Science, Tohoku University
2-1-1 Katahira, Aoba-ku, Sendai, Miyagi 980-8577, Japan
Phone: +81-22-217-5240 E-mail: Samukawa@ifs.tohoku.ac.jp
[2]National Institute of Advanced Industrial Science and Technology
2-13 Tsukuba Central, Umezono, Tsukuba, Ibaraki 305-8568, Japan

1. Introduction

The scaling down of MOSFETs requires gate length less than 35 nm[1]. In this generation of the devices, it is difficult to improve performance of MOSFET devices by only down-scaling because of short channel effect. To solve these problems, the new MOSFET structures, such as FinFETs and surrounding gate transistor (SGT), has been widely investigated. However, when conventional plasma etching and thermal oxidation are applied to these new proposals, some fatal problems occur. For example, electrical property of devices degrades because of UV damage and charge up during the plasma etching process and diffusion of dopant during high temperature process of conventional thermal oxidation (> 800 ºC). On the other hand, it is difficult to fabricate gate dielectric film and insulating film of SGT independently[2] due to the isotropic oxidation of conventional thermal oxidation. Furthermore, three dimensional transistor, (which needs uniformly-sized film dimensionally, was not fabricated due to the oxidation rate varies with the lattice plane of Si[3]) this sentence is not easy to understand. As mentioned above, it is difficult to meet these requirements by using conventional thermal oxidation methods. Therefore, a novel oxidation method with features of low temperature, anisotropic oxidation and independence from silicon lattice plane is necessary.

To breakthrough these problems, we proposed the neutral beam (NB) process as an alternative to the plasma etching process and thermal oxidation process. We have already used neutral beam etching (NBE) and conventional thermal oxidation process to fabricate three-terminal FinFETs and improved its performance[4]. Also, we have developed the fabrication of fine and ultra thin SiO_2 film by using our developed damage-free neutral beam oxidation (NBO) at low temperature of less than 300 ºC[5,6]. In this study, we fabricated three-terminal FinFETs and its gate dielectric film and fin were formed by NBO and NBE, respectively. We compared the electric properties of FinFETs using NBO process with that using conventional thermal oxidation process.

2. Experimental

SiO_2 films were formed using our developed NBO (hereafter the SiO_2 film is called NBO film) and the detailed characteristic of NBO was described in elsewhere[5]. The bombardment of the oxygen neutral beams with energy smaller than 10eV activates the surface atomic layer of Si and the atomic layer oxidation process effectively progresses even at a low temperature of about 300ºC. The pressure in process chamber was fixed at 0.14 Pa.

Figure 1 shows the schematic process flow of FinFETs and the details was described in elsewhere[4]. Here we briefly described the procedures. Silicon on insulator (SOI) wafer was used to investigate the FinFETs with n-channel. The pattern for fin structure was determined by electron beam (EB) lithography and then the fin structure was fabricated by NBE. After that, NBO film was grown on the sidewall of the fin structure. Gate dielectric film was covered with n+ polycrystalline-Si (Poly-Si). After gate electrode formation using inductive coupled plasma (ICP), ion-implantation (P) into the extension of the source/drain (S/D) was performed. S/D was activated at 950ºC for 2 seconds. Then the aluminum electrode metallization was fabricated. Finally, the devices were sintered at 450ºC in 3% H2 ambient.

Single and multi FinFET were fabricated on the same wafer. Figure 2 shows the schematic illustrations of both FinFETs. The main dimensions of single FinFET are as follows: gate length L_g =160nm, fin thickness T_{fin}=80nm, fin height H_{fin}=100nm. The multi FinFET has 45-fins, and the main dimensions of it are as follows: gate length L_g =20μm, fin thickness T_{fin} =100nm, gate electrode area A =180μm.

We evaluated the electrical properties of FinFETs using a prober and KEITHLEY 4200 at room temperature in air.

3. Results and discussions

Figure 3 shows the cross-sectional TEM image of fin oxidized by using NBO tilted at 60 degrees. It was shown that the surface of the fin was oxidized uniformly. This result indicated that NBO is anisotropic oxidation. The detailed anisotropic of NBO process was described in elsewhere[7].

I_d-V_g, C-V and gate leakage current of the fabricated FinFETs were measured. Because the gate electrode of single FinFET is too small, only multi FinFETs were used for C-V characteristic. It clearly shows that the longer NBO irradiation time is, the lower off current and the more reduction gate leakage current are. These results were speculated that the off current and the gate leakage current depend on SiO_2 film thickness. Therefore, we calculated equivalent oxide thickness (EOT) from C-V characteristic (Figure 4(b)) and gate electrode area because the gate NBO

film thickness is too difficult to measure. The EOT of the NBO film with irradiation of 250, 500, 1000 and 2000 seconds are 2.01, 2.17, 2.47 and 2.64, respectively. This result shows that off current and leakage current depend on EOT of the NBO film. These results show that the multi FinFETs had the typical characteristic of transistor.

In order to compare the fabricated FinFETs using conventional thermal oxidation process with that using NBO process, we measured I_d-V_g characteristic of single FinFETs as shown in Figure 5. The S value of the FinFET fabricated by NBO was apparently improved as compared with the one by conventional thermal oxidation. The dimensions of the FinFET fabricated by conventional thermal oxidation are as follows: gate length L_g =110nm, fin thickness T_{fin} =50nm, fin height H_{fin} =100nm. Therefore, if the FinFET is fabricated by NBO with the same dimensions, the S value may be greatly improved. We also calculated effective mobility of the multi FinFETs as shown in Figure 6. This result shows that the effective mobility of the multi FinFETs fabricated by NBO process was improved in high carrier density area. It is speculated that the residual stress of the FinFET fabricated by NBO process is smaller than that by thermal oxidation process due to the uniform film on the fin side wall.

4. Conclusions

We have fabricated very thin gate SiO_2 film by using our developed NBO technique at low temperature of 300ºC. Electrical property of single FinFETs and multi FinFETs fabricated by NBE and NBO was investigated. I_d-V_g, C-V and gate leakage current characteristic showed that FinFET had a transistor property. Moreover, S value of the FinFET fabricated by NBO process was apparently improved. The improvement of effective mobility of the multi FinFETs fabricated by NBO process was more than that by NBE and thermal oxidation process. These results greatly support the great potential of NB technology on nanoscale devices.

References

[1] International Technology Roadmap for Semiconductors 2008.

[2] I De, et al., Solid-State Electronics, Volume 44, Issue 6, 1 June 2000, Pages 1077-1080

[3] F.H.Yuan, et al., Surface and Coatings Technology, Volume 183, Issue 1, 1 May 2004, Pages 106-110

[4] K.Endo, etal, IEEE, Volume53, NO.8, AUGUST 2006, Pages1826- 1833

[5] T.Ikoma, et al., SSDM (2006), Yokohama, pp.448-449

[6] M.Yonemoto, et al., SSDM(2008),Tshukuba,pp.340-34

[7] M.Yonemoto, et al., Jpn. J. Appl. Phys, 48 (2009)

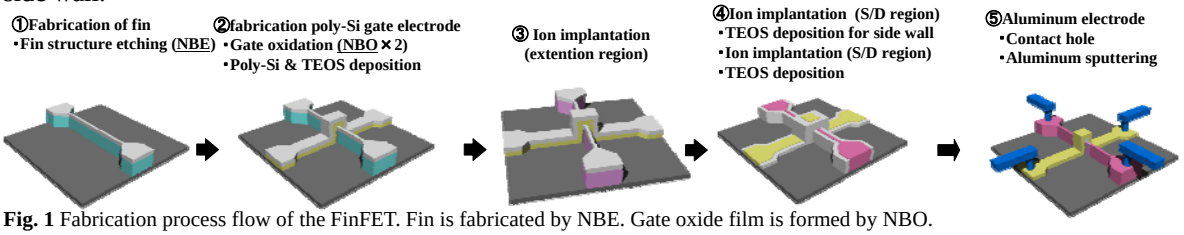
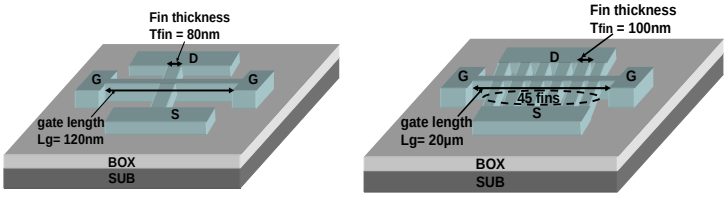


Fig. 1 Fabrication process flow of the FinFET. Fin is fabricated by NBE. Gate oxide film is formed by NBO.



(a) single FinFET **(b) multi FinFET**

Fig. 2 Schematic illustrations of (a) single FinFET and (b) multi FinFET

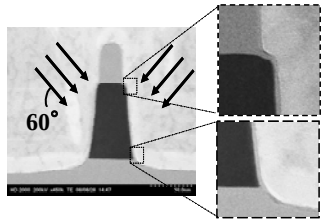


Fig. 3 Cross-sectional TEM image of fin oxidized by using NBO

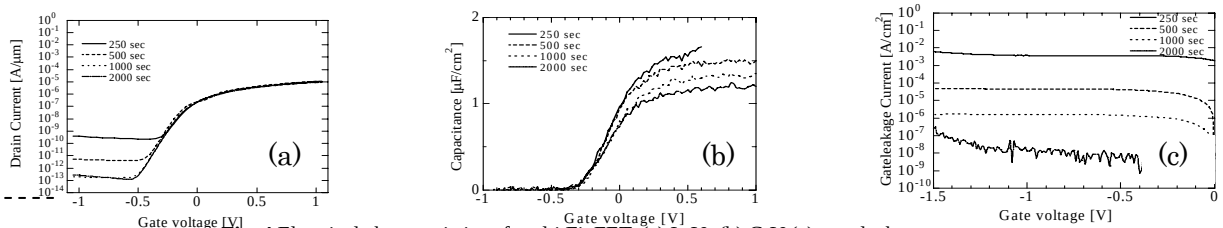


Fig. 4 Electrical characteristics of multi FinFET. (a) I_d-V_g (b) C-V (c) gate leakage current

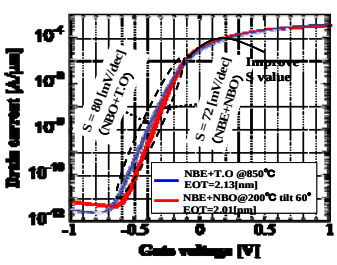


Fig. 5 I_d-V_g characteristic of single FinFET

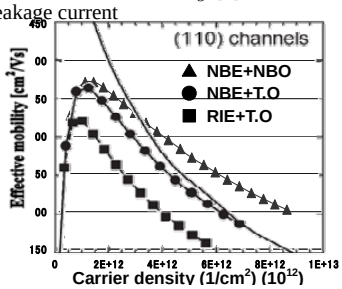


Fig. 6 Effective mobility of multi FinFET